



A MULTI-CHANNEL DIGITAL TELEMETRY SYSTEM  
FOR LOW FREQUENCY DATA

BY

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ABSTRACT

An inexpensive general purpose digital telemetry system for collection of low frequency geophysical data from U.S. Geological Survey instruments (eg. tilt, strain, gravity, creep, water level, radon, magnetic field, resistivity, telluric current, temperature, etc.) has been designed and built. This system provides data for a more general interactive data acquisition, retrieval and analysis system. The field stations are self-contained, battery operated and housed in weather proof containers. Each accepts up to 15 analog data inputs in the range of -5 to +5 volts. The dynamic range is 70db.

The units transmit information as FSK (Frequency Shift Keyed) tones onto either a phone line or radio link with up to 150 transmitters sharing one line. The average power consumption is  $0.06 nR$  watts where  $n$  is the number of input channels transmitted and  $R$  is the sample rate in minutes<sup>-1</sup>.

The central receiver-recorder unit accepts and decodes the FSK tones and converts, formats and records the digital data together with time information and station identification on IBM compatible magnetic tape. The digital data are also converted and recorded in analog form for visual monitoring.

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## I. INTRODUCTION

Serious attempts at predicting earthquakes require for their basis, "real time" data that is both readily accessible and error free. Low frequency geophysical data such as tilt, strain, magnetic field variations, etc., may provide direct measurements of deformations preceding earthquakes. These deformations usually have long time scales. Analog telemetry systems can be used to collect these data; however, due to noise, limited dynamic range, system drift and deviations in linearity and gain, tectonically related observations cannot be unambiguously identified. These problems are avoided by using digital telemetry techniques. In such schemes the signal at the site is transformed and transmitted as coded tones. Telemetry noise in this case results in missing data rather than spurious signals.

Digital data acquisition systems have been designed for many purposes although usually for high data rates. For geophysical purposes, economy, low data rates, time sharing of coupling medium and options for using several different coupling mediums simultaneously are the prime design requirements. The generation of standard I.B.M. computer compatible magnetic tapes or accessible memory storage as the primary data output avoids developing dedicated computers and associated hardware and, as a convenient pivot point, allows development of more general computer-based data retrieval and analysis systems for which the low frequency data system would provide just one such input.

The digital telemetry system described here consists basically of two separately functioning systems, the field units and the central receiver-recorder system, coupled either by telephone lines or radio or a mixture of both. A block diagram of the system is shown in Figure 1.



The fundamental components for the system are commercial encoder/decoder modems used first to telemeter binary-coded-decimal (B.C.D.) data from proton magnetometer field installations (Smith et al., 1973). Adaptation of this system to accept, convert, transmit, and receive analog data was completed by Rex Allen (1976). For the purposes of completeness, description of the relevant parts of Allen's transmitter and receiver are included, where necessary, in this report.

ACKNOWLEDGEMENTS

Many individuals were involved in various phases of the preparation and initial review of the material presented in this report. Contributions have ranged from re-checking the parts list and re-drawing figures to suggestions on electronic design and hardware configurations. Bob Mueller, James Chan, Steve Gallantine, Marty Varon, Kent Peterson, Vince Keller, and others have made significant contributions.

## II. SYSTEM DESIGN CONSIDERATIONS

The principal design constraints for the system were:

1. Low-power field transmitter.
2. Efficient use of phone lines, i.e., line sharing rather than dedicated lines for each data input (phone line leasing is the largest single continuing cost for remote data retrieval).
3. Reliability - Proven field tested commercial subunits such as data encoders (LARSE), incremental tape recorders (CIPHER), etc., were used in preference to more recent state-of-the-art designs.
4. Simplicity - for both easy field and laboratory trouble shooting.

The concept of subdividing a phone line into a number of discrete channels and multiplexing onto line only during the transmission time satisfies the requirement of efficient use of the phone line. The average power of the field transmitter can be made very low if the system is shut down at all times except just prior to and during transmission and if the transmission time is short compared with the interval between samples. Unfortunately the transmission time is a function of the channel bandwidth required to transmit the FSK tone information. Very rapid transmission times and imply high data rates <sup>and</sup> large channel bandwidths and therefore fewer channels per phone line. This conflicts with the requirement for efficient phone line use by increasing phone line costs. A compromise must be made between channel width, transmission time, number of instruments, and sample rate. Fortunately, however, for most low frequency geophysical data needs, a sample every 10 minutes or longer is quite adequate (see Table 1) particularly if continuous on-site analog recordings are also made.

TABLE 1: Data rates for various instruments

<u>Instrument</u>	<u>Typical rate: 1 message per</u>	<u>Min reasonable rate: 1 message per</u>	<u>Max reasonable rate; 1 message per</u>	<u>Words per message</u>	<u>Bits per word</u>
Creepmeters	1 hour	12 hr	1 min	1	12
Magnetometers	1 min	10 min	1 sec	1	12
Radon sensors	1 hour	12 hours	10 min	1	12
Resistivity	10 min	1 hr avg	10 min avg	1	12
Sea-level	10 min	1 hr	10 min	1	12
Strain meters	10 min	10 min	1 sec	1	12
Telluric current	10 min	1 hr avg	10 min avg	1	12
Tiltmeters	10 min	10 min	1 sec	2	12
Water-level	1 hr	12 hr	10 min	1	12
Water-temperature	1 hr	12 hr	1 hr	1	12

### III. SYSTEM DETAILS

#### A. Field Transmitter

A block diagram of the field transmitter is shown in Figure 2. The essential elements are:

1. Multiplexer and power control circuitry
2. Analog to digital converter (ADC) and parallel to serial converter
3. Clock
4. Voltage controlled oscillator
5. DC - DC converter (power supply)

Following the design details described in Allen (1976), the field transmitter accepts 1 to 15 analog inputs. A CMOS clock powers up the system and after a short delay to allow for circuit stabilization the first analog input is digitized with a 12 bit analog to digital converter. The 12 data bits together with a 4 bit input identification code (ID) are converted to serial form by a parallel to serial converter (LARSE). The modem takes the 16-bit word, interleaves it with preamble and other information required for word-asynchronous operation, and outputs a serial code. This code is transmitted by a FSK crystal reference voltage controlled oscillator and line driver via telephone lines or radio links to the data collection points.

Subsequent channels are transmitted in sequence until reaching the last preselected channel. The field unit then switches off and waits for the next "go" command. During standby, power is applied only to one CMOS package and to the sample interval clock if an internal clock card is being used. The average power consumption is  $0.06 n R$  watts,  $n$  being the number of input channels transmitted and  $R$  the sample rate in minutes<sup>-1</sup>.

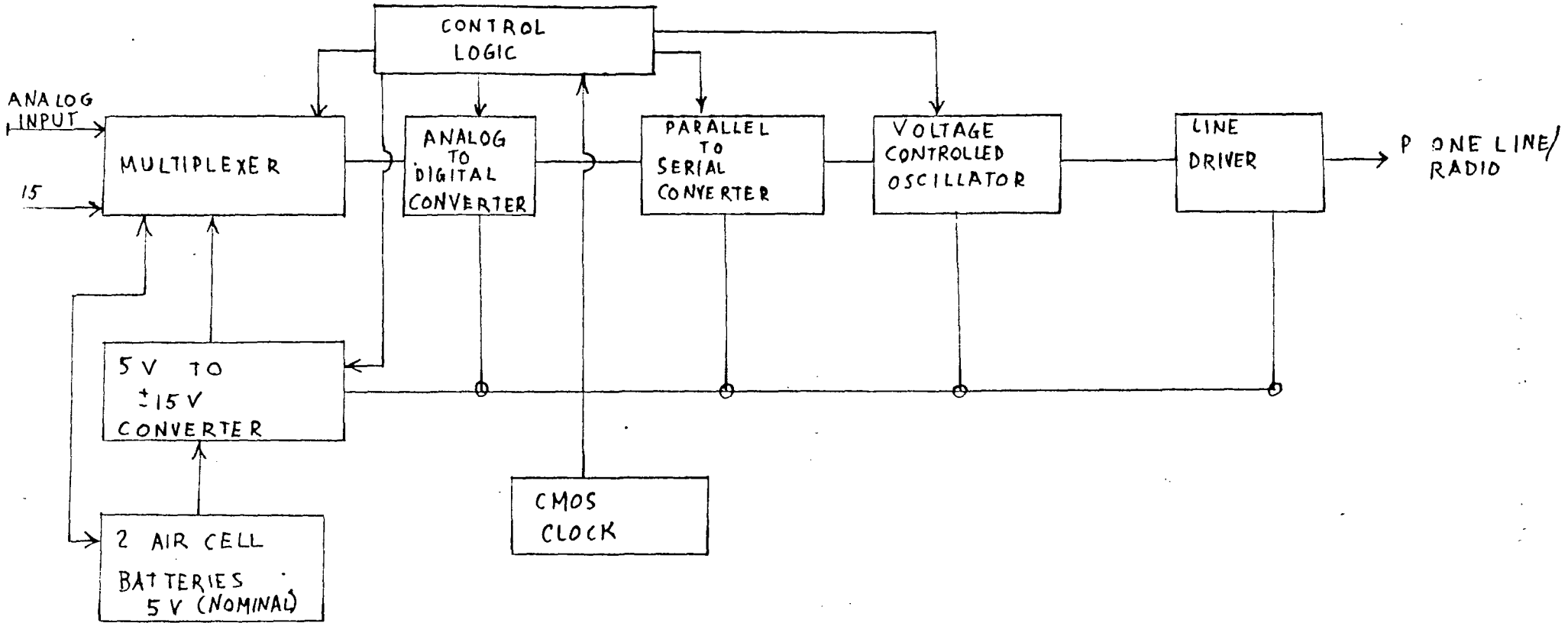


Figure 2: Block Diagram of Digital Field Transmitter.

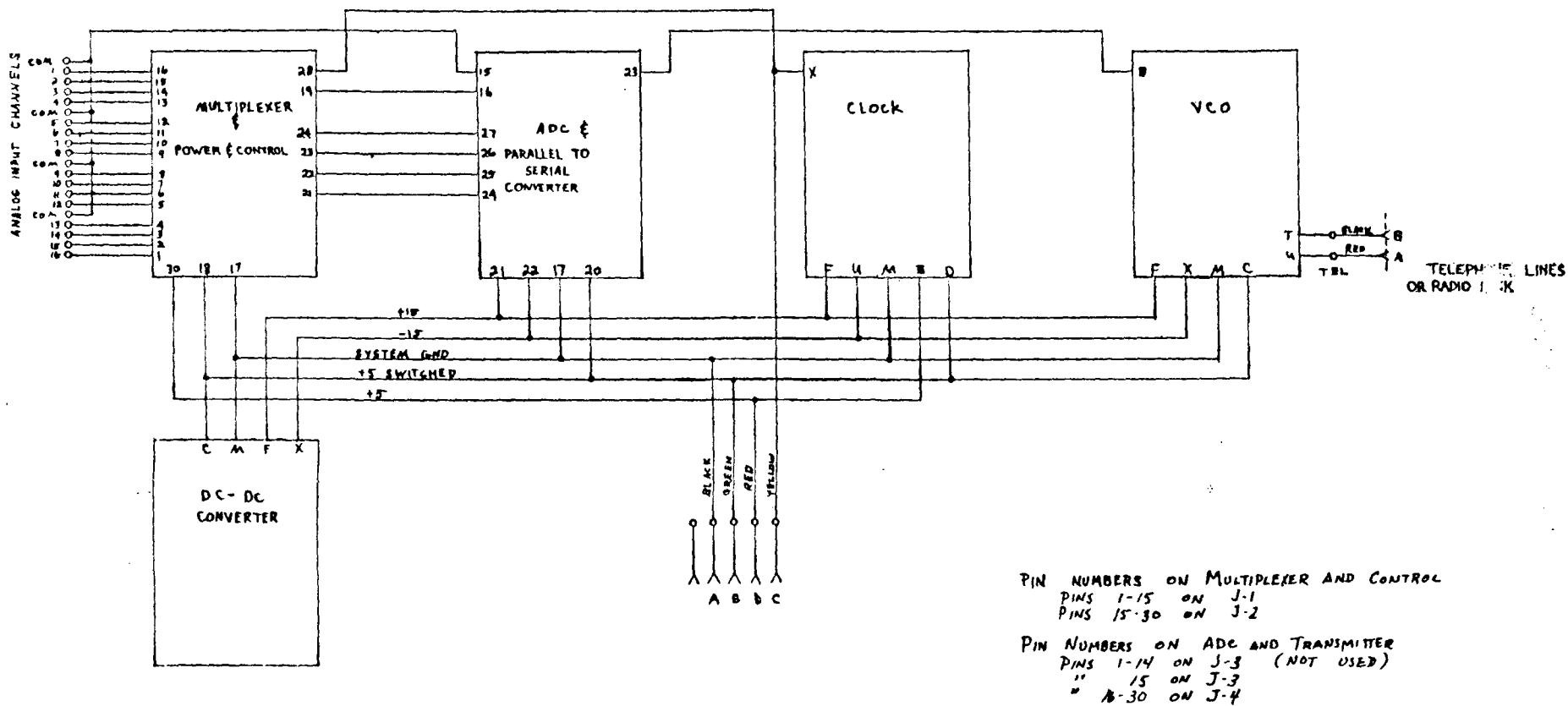


Figure 3: Mother Board Circuit Card for Digital Field Transmitter. (After R. Allen)

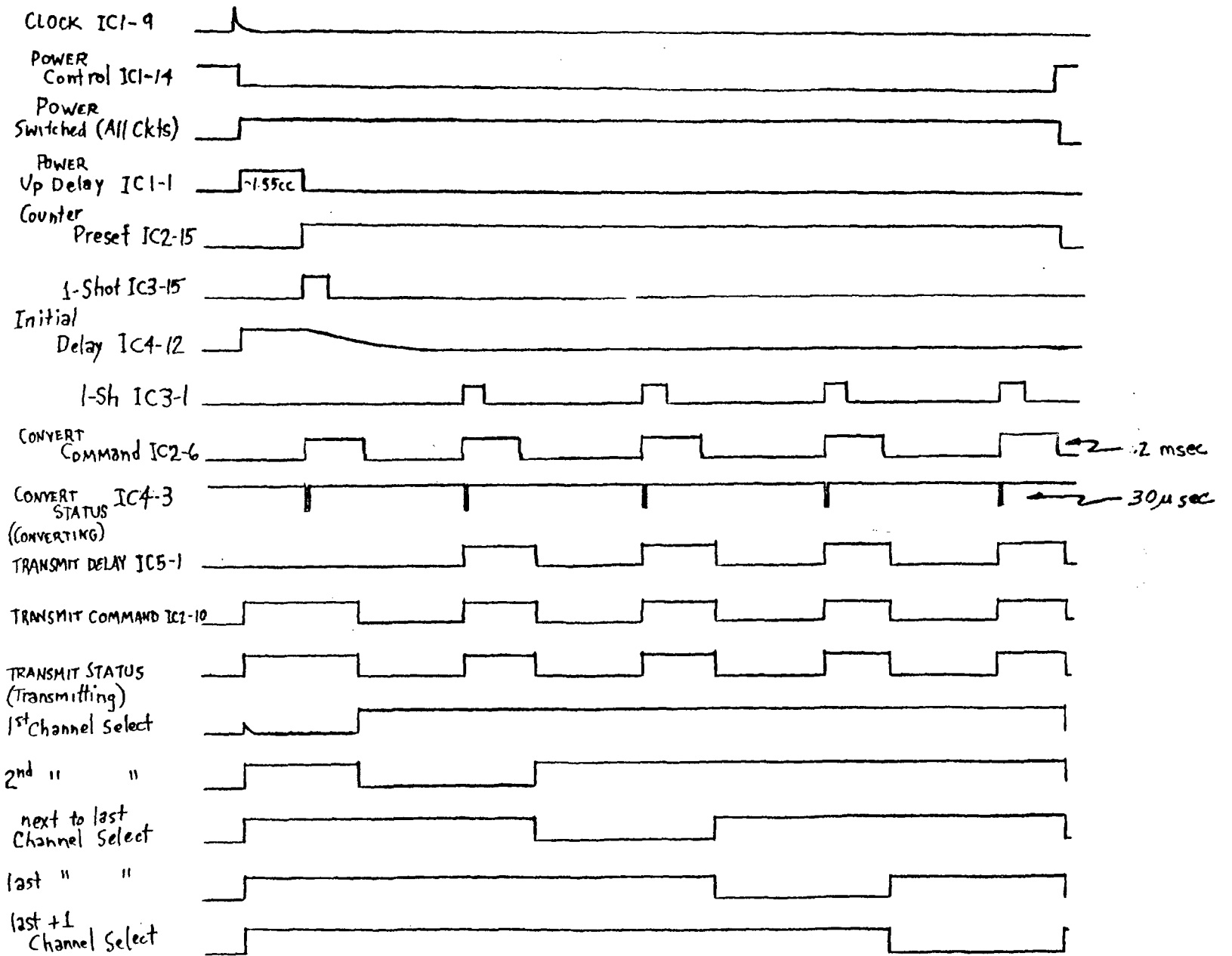


Figure 4b: Timing Diagram for the Multiplexer Signal and Power Control Card. (After R. Allen)



A more detailed circuit diagram that corresponds to the actual cards in the field unit "mother board" circuit is shown in Figure 3. Each section of this figure corresponds to "plug in" circuit cards which will be discussed in order in the following sections. The step by step operation of the complete system is discussed in section A.6.

#### A 1. Multiplexer, power and signal control

The detailed circuit diagram of this card is shown in Figure 4a. The power-up command from the clock changes the state of the first J-K flip-flop in IC1. This switches on the power transistor 2N5974 and power is supplied to all the circuit cards except the clock. A second J-K flip-flop in IC1 is set to operate as a multivibrator and, after being switched on, feeds a binary counter IC6 whose initial state is pre-set. The multivibrator output is also delayed and used to control the start of the analog to digital conversion and data transmission. Starting from its pre-set state the binary counter is fed into a 4 bit decoder (IC7). The parallel input data are fed to a series of reed relays. Starting from the relay corresponding to the preset state of the binary counter the input data are sequentially switched to the output data line. A preselected connection from the decoder outputs corresponding to the last input data to be transmitted and resets the power up J-K Flip-Flop/shuts the transmitter off. Details on how to preselect the first and last data channels to be transmitted are covered in the next section. The timing diagram for the operation of the multiplexer and power control circuitry card is shown in Figure 4b.

#### Program Plug

Any number from 1 to 15 consecutive data inputs may be transmitted by means of a program plug which initiates by presetting the multiplexer,

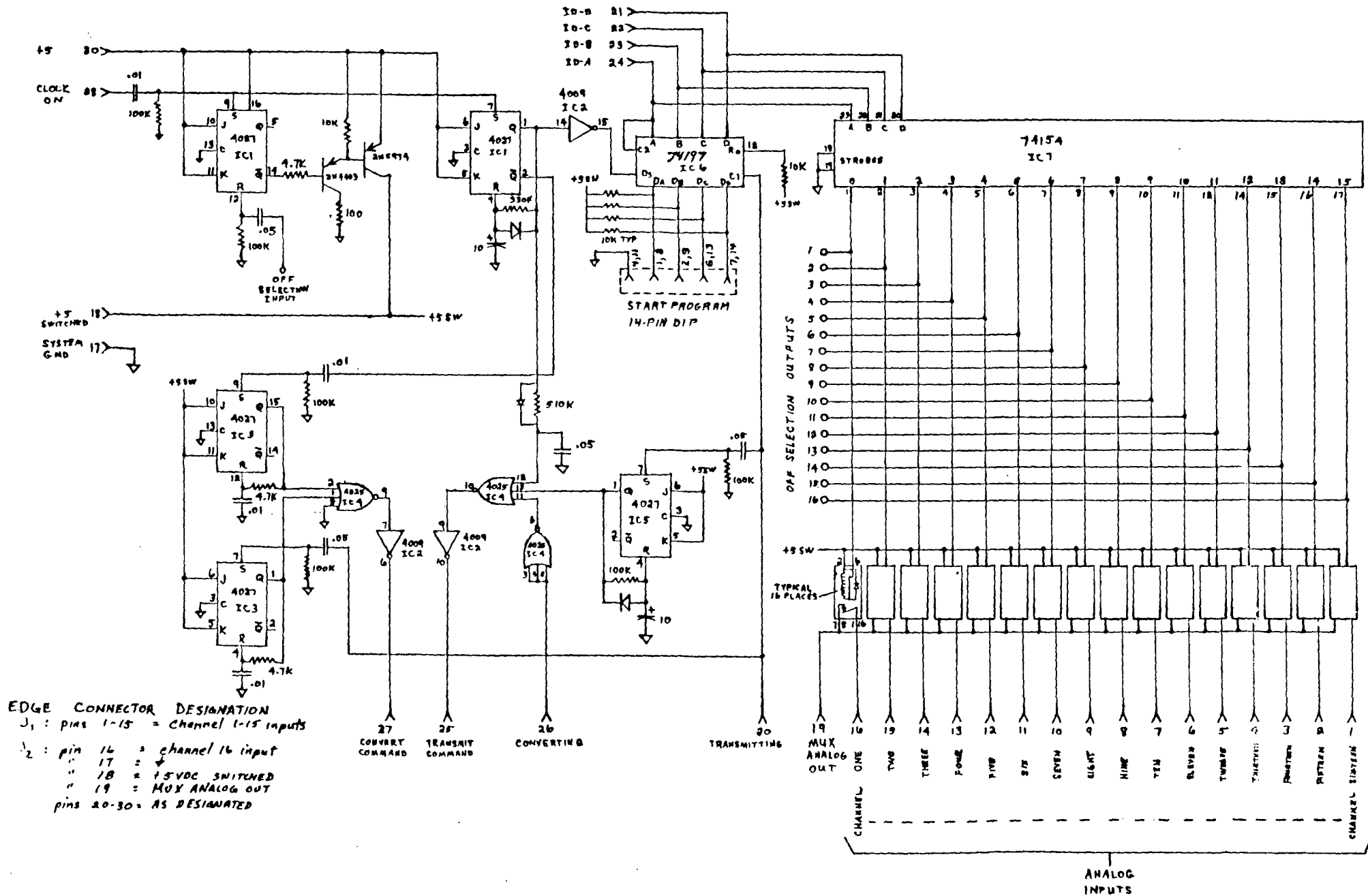


Figure 4a: Circuit diagram of the Multiplexer Signal and Power Control Card. (After R. Allen)

the first channel to be transmitted. The program plug fits into a 14-pin DIP socket on the multiplex and control board. The multiplexer may be preset to any value from 1 to 16 by appropriate hard wire ground connections to the pins on the plug. Table 1a lists the pins to be grounded for initiation of transmission from each of the input data channel numbers. The last input transmitted is determined by a preselected shutdown control.

An example may clarify how to program the transmitter to transmit the desired channel(s). Suppose it is desired to start transmission on channel 7, then we set the plug for 6<sub>16</sub> which means we ground pins 1 and 7.

The last data channel transmitted depends on the preselected shutdown control. The position of a jumper to the off select pin corresponding to this channel will result in a power shutdown when the multiplexer accesses this channel. Continuing the previous example, if transmission was started on 7 and we desire to stop on 9 (transmit 7, 8), then the OFF-select jumper wire should be connected to pin 9 of the 16 off-select pins.

In the present system channel 16 is not used. If however, the transmitter is programmed to transmit starting at, for example, channel 13 and stopping at channel 13, then 16 will be transmitted, followed by channels 1, 2 and 3. No harm will be done, but channel 16 will be loaded into receiver backplane Dip #1 and this data is not recorded on the cipher, but an analog record is available if desired.

TABLE 1a. PROGRAM PLUG CONNECTIONS

Input Data Channel Number Initially Transmitted	Program Plug Pins * Connected To Ground
1	1, 2, 6, 7
2	2, 6, 7
3	1, 6, 7
4	6, 7
5	1, 2, 7
6	2, 7
7	1, 7
8	7
9	1, 2, 6
10	2, 6
11	1, 6
12	6
13	1, 2
14	2
15	1
16	

\* Note: Pin 1 is internally connected to pin 8, pin 2 is connected to pin 9, pin 6 to pin 13 and pin 7 to pin 14

Pins 4, 11 are ground. Pins 3, 5, 10, 12 are not connected.

A.2 Analog to Digital Conversion (ADC), parallel  
to serial converter and data transmission checks

The details of the circuitry for the transmitter card are shown on the diagram in Figure 5. Analog data from the multiplexer card are switched through a buffer (LM 310N) to a 12 bit A-D converter. The parallel binary output of the A-D is the input of the parallel to serial converter. This unit (LARSE SEN modem) is the most complex component of the field transmitter since as well as serializing and controlling the data transmission rate, it inserts redundant check bits in the serial data which allow for checks to determine whether a correct transmission of the data has been completed.

The particular operation selected for the modem used in the field transmitter configuration are for 5 volt logic input, 60 bits per second data rate and "single word double scan security". This scheme in addition to other checks described in the receiver section provides system security against erroneous transmissions. Each word consists of data and synchronization bits. This is also described in the receiver section of this report. The serial data train, then feeds to the voltage controlled oscillator (VCO) and line driver card.

A.3 CMOS Clock

The CMOS random clock provides the turn on pulse for the transmitter. Its circuit diagram is shown in Figure 5a. The random nature of the clock is its single most important feature since on

shared lines the probability of any two clocks being coincident for any length of time is small (<10%). Since in most applications random intervals between samples of from 0.5 to 20 minutes are desired, the clock has a number of possible outputs. These derive from a 14 stage divider. For example, for an oscillator frequency of 13.6 Hz, intervals between samples of 37.5 sec 1.25 min, 2.5 min, 5 min, 10 min and 20 min are possible. Power to the clock is 60 $\mu$  watts or 12 $\mu$ A at 5 V. Since the transmitter is normally off, this current (20 ma) is also the primary current drawn by the whole system for sample intervals greater than 5 minutes. If the input voltage to the transmitter is reversed accidentally, only the clock will be destroyed, since all other circuits are disconnected from the power supply except during transmission.

The clock itself consists of two sections: an RC oscillator and a divider section. The oscillator frequency is given by

$$f = \frac{1}{2RC}$$

f is the frequency of the oscillator section and R and C are indicated on Figure 5a. For example, in our application C=0.04MF R = 1.0 M $\Omega$  which results in an output square wave of approximately 13 Hz. When divided by 2<sup>14</sup> (the 14 stage of the 4020 shift register) this gives a square wave of period approximately 20 min. Other binary sub-multiples of this period can be easily selected.

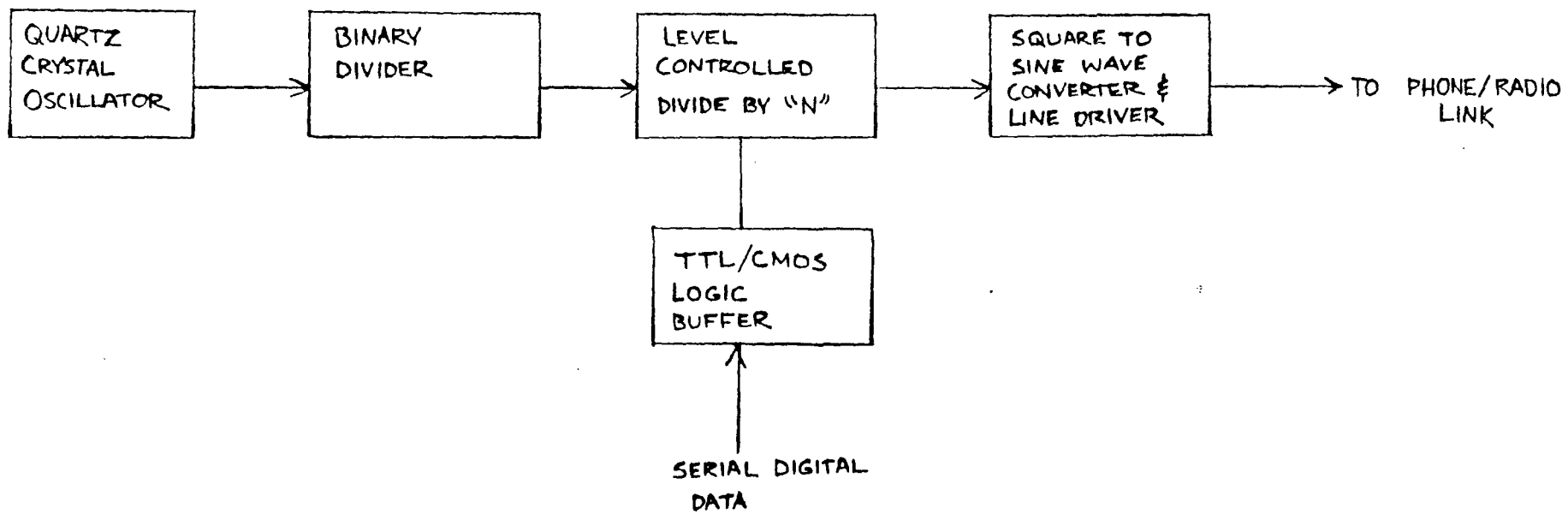


Figure 6: Block Diagram of Quartz Crystal Reference Digital VCO.

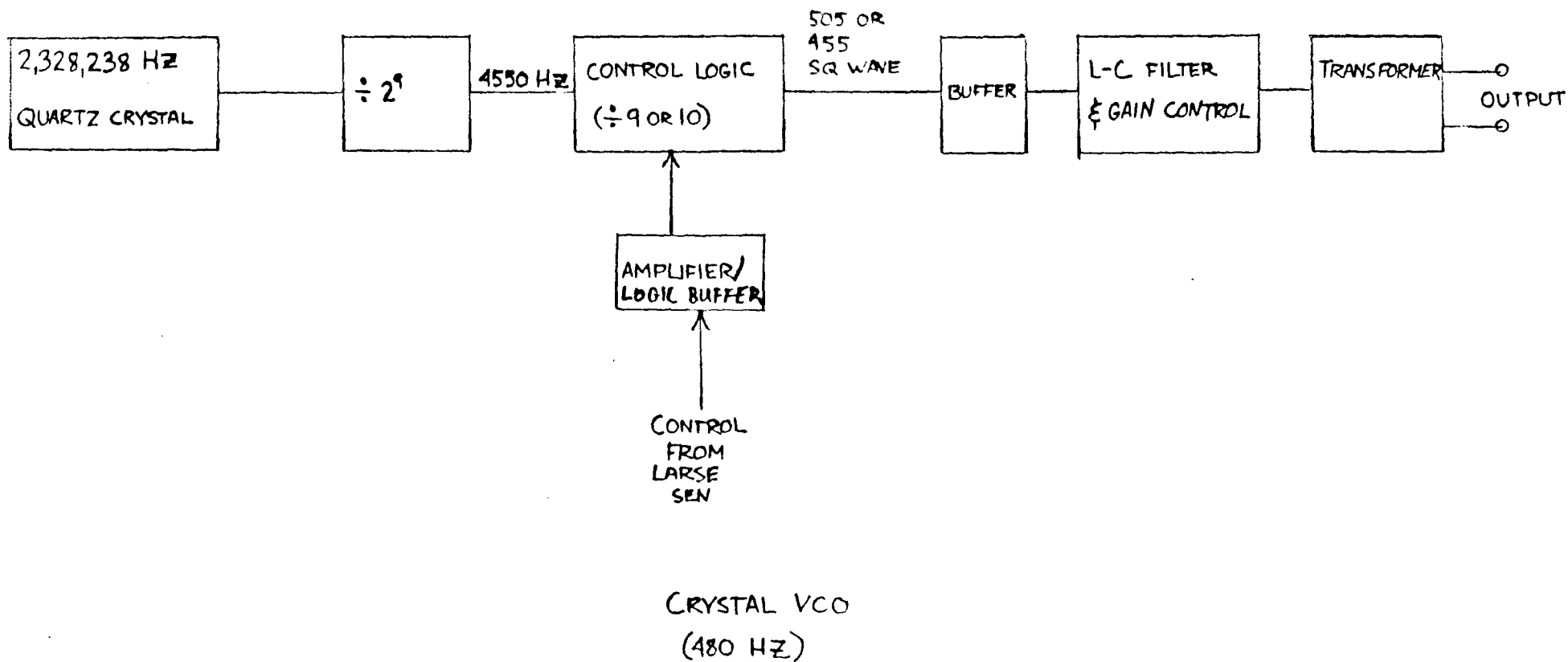


Figure 6a: Block Diagram of VCO for 480 Hz.



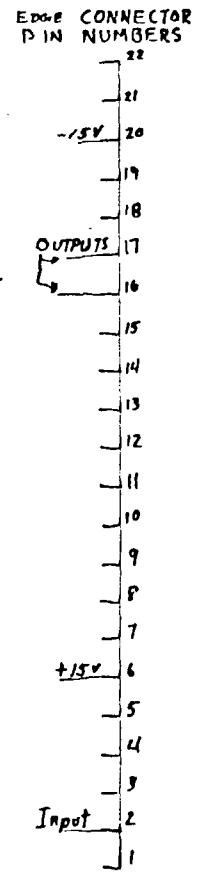
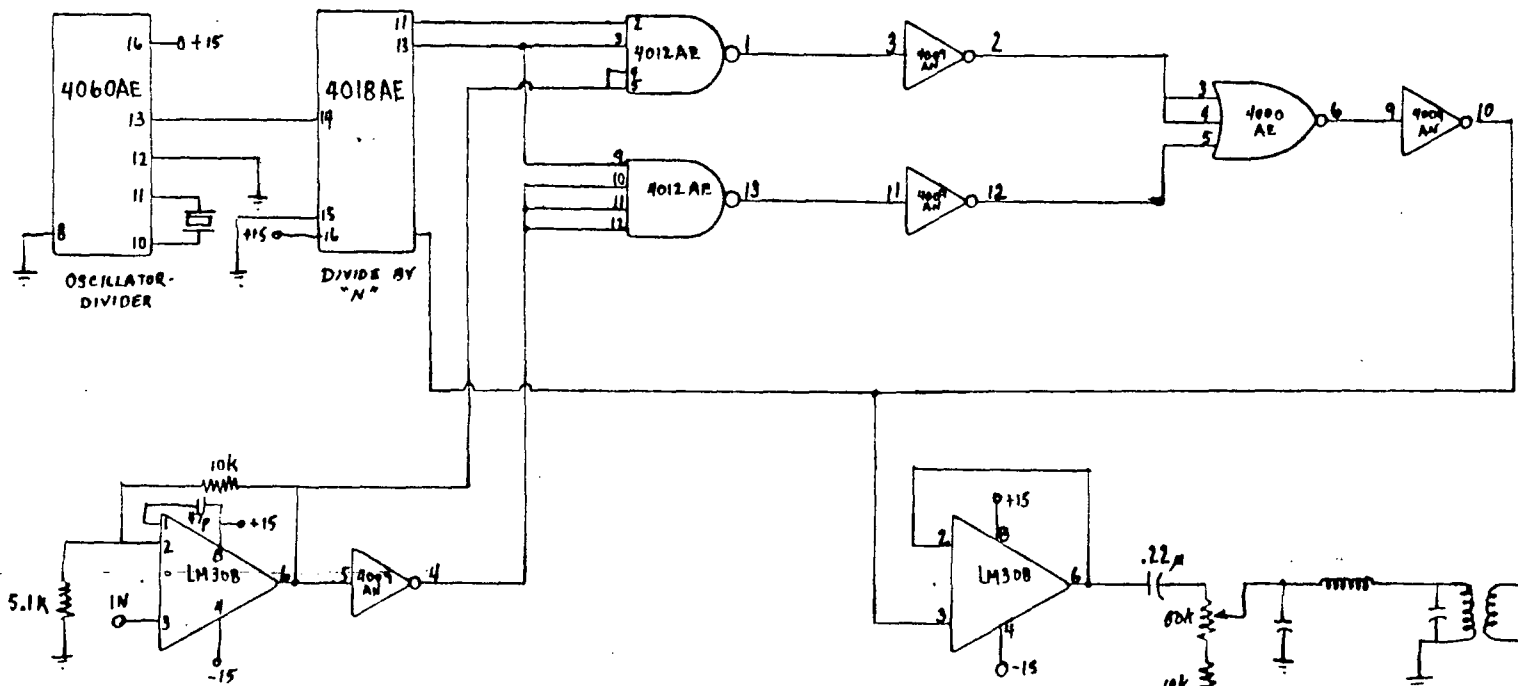


Figure 7: Circuit Diagram of Quartz Crystal Reference Digital VCO.

(fm LARGE-SEN,  
0-5 V)

#### A.4 Voltage controlled Oscillator (VCO)

The block diagram of the digital VCO is shown in Figure 6. The crystal frequency is divided by  $2^n$ ,  $n$  being a function of the number of stages of the counter used. The output of this binary counter feeds the input of a "divide by N" counter ( $N=2,3\dots 10$ ). The division depends on the feedback used. The feedback is changed using standard gating techniques and depends on whether the serial data inputs are high or low.

A detailed circuit diagram of the digital V.C.O. set up for output frequencies of 455 and 505 Hz is shown in Figure 7.

These frequencies, i.e. around 480Hz, are the primary ones transmitted at present from existing field sites in California. The crystal oscillator and the primary  $2^9$  binary division is achieved on one CMOS integrated circuit (CD4060). The input logic levels are gated (CD4012, 4009) into a "divide by N" integrated circuit (CD4018) so as to divide by 9 for a high level or 10 for a low. A micropower operational amplifier (LM308) converts the TTL logic levels (5V logic) to CMOS logic levels (15 V logic). For a high input, division by nine is performed by feeding back the Boolean product of pins 13 and 11. For low input only pin 13 is fed back. It is clear that some combinations of frequencies and bandwidths are not possible with this system. In such cases the same basic digital VCO can be used with a different number of binary divider stages in combination with the "divide by N" section to produce the required frequencies and bandwidth, if N can be properly selected. The two possible output frequencies are then driven down the phone line.

The output of the CD 4018, a square wave whose frequency depends on the data input level, is fed to the input of a buffer (micropower LM308 op amp). The buffer is voltage divided and filtered by the LC bandpass filter into a step down transformer with 600 ohm output impedance for maximum power transfer to the phone line. With the present dividing scheme the crystal frequency can be calculated from the following relationship:

$$f = 4850.53 \frac{(f_L + f_H)^*}{2}$$

For example, for a 480 Hz channel with  $f_L = 455$  Hz;  $f_H = 505$  Hz;  $f = 2.328$ M Hz. When this frequency is divided by  $2^9$  and by either 9 or 10 the values of  $f_L$  and  $f_H$  can be checked. In the above example  $f_L$  and  $f_H$  are within 0.5 Hz of the required values of 455 and 505 Hz respectively.

#### Crystal VCO Specifications

Power:  $\pm 15$ v @ 6 to 8 ma

Stability for 5M Hz crystal: Less than 1.0 Hz change over  $-30^\circ$  C to  $+60^\circ$  C

Output: Sine wave, +1 db max into 600 $\Omega$  load

Long term drift:  $\leq 0.2$  Hz

A component location diagram is found in Appendix B-2.

\*  $f_L$  and  $f_H$  are the band edge frequencies

### A.5 DC/DC Converter

In order that the field units operate from low voltage, large capacity (1000 amp-hr) batteries, a DC/DC converter is employed to supply the  $\pm 15$ -volt power to circuits such as, for example, the ADC, LARSE SEN unit, operational amplifiers, etc. The efficiency is approximately 65% (300 ma total) at 5 volt and full load with 0.1% voltage regulation for  $\pm 5\%$  input voltage change.

To prevent damage from incorrect polarity to the DC/DC converter module a diode-reed relay protection scheme is used (Figure 8). If the voltage polarity is reversed the diode becomes conducting. This opens the relay contacts and disconnects power from the MP 3020. The protection circuit with correct battery polarity is also shown in Figure 8.

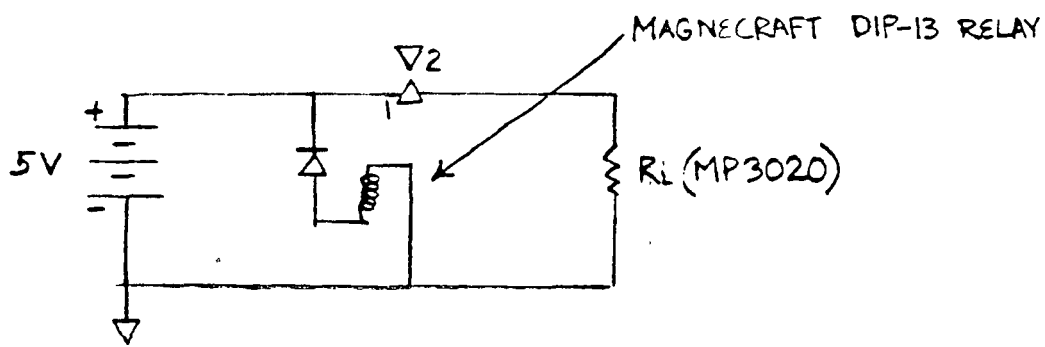
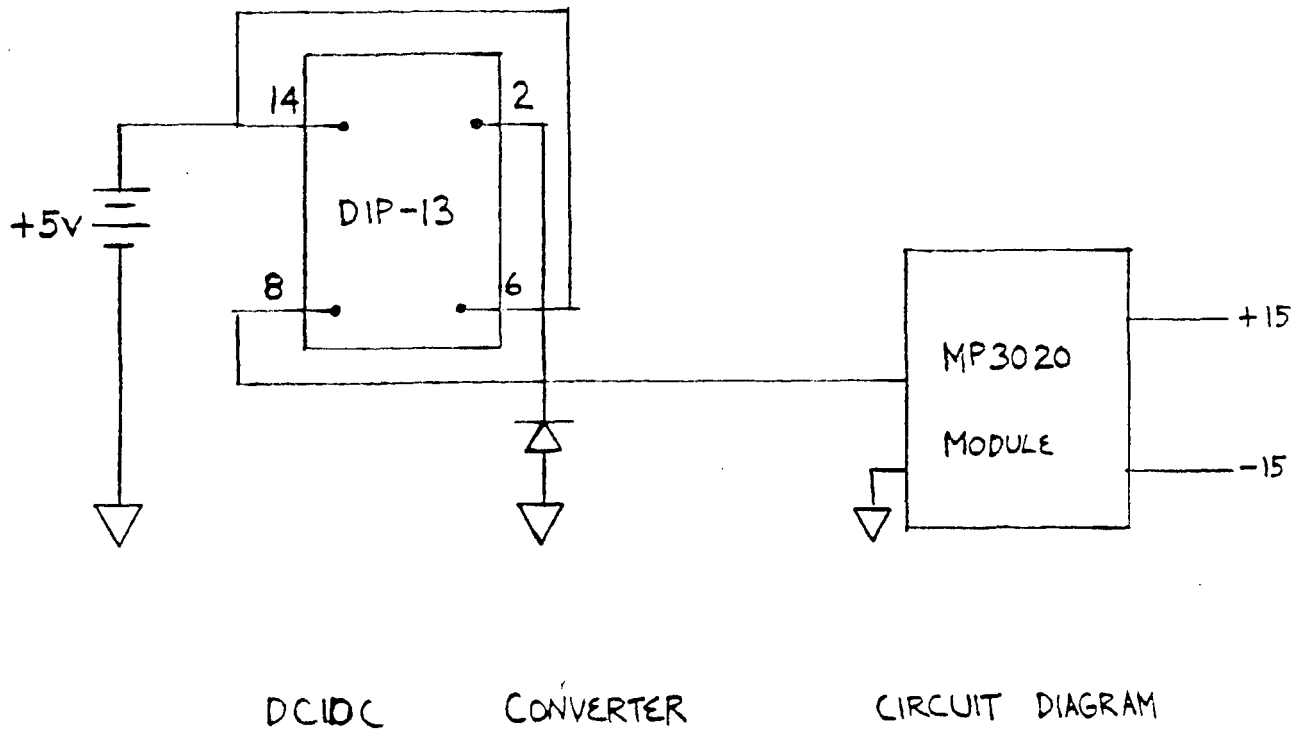


Figure 8: Reverse Polarity Protection Circuit and DC/DC Converter Circuit Diagram.

#### A.6 Step by Step operation summary of field transmitter. (1)

The operation of the field transmitter starts with a clock pulse.

1. A "Clock-On" positive transition sets the Power Control and Power-Up Delay FF's at IC 1-9,7. This applies 5 volts to all circuits including the DC-DC converter which in turn supplies +15 v to those circuits requiring it. During Power-Up Delay the sequence counter is preset by IC 2-15 to the starting value selected by the programming plug. The analog voltage from the pre-selected first channel is being applied to the input buffer and ADC during Power Up.
2. Power-Up Delay times out and the positive transition at IC 1-2 sets the Initial 1-shot IC 3-15.
3. A convert command for the ADC is generated at IC 2-6.  
NOTE: The Initial Delay circuit at IC 4-12 prevents generation of spurious Transmit Command pulses at Power On (step 1) and at time-out of Power-Up Delay (step 2).
4. Convert Status (Converting) goes low at IC 4-3, indicating that the ADC is busy.
5. When conversion is complete Convert Status goes high and Transmit Command goes low at IC 2-10, initiating a data word transmission from the Larse modem after IC 4-12 goes low.
6. Transmit Status (Transmitting) goes low at the start of transmission, incrementing the sequence counter. Note that the two FF's are not set by the negative pulse at IC 3-7 and IC 5-7. The transmitter continues to transmit the digital information from the ADC and also the ID bits which are now being shown by the sequence counter.

Notice that these are the ID bits for the second selected channel, not the first. The decoded channel select has now enabled the second channel and this analog voltage is being fed to the input buffer for the entire duration of transmission of the preceding channel.

7. The channel transmission finishes and Transmit Status goes high. This sets Transmit Delay IC 5-1 disabling Transmit Command until the Transmit Delay FF has timed out. Continuing 1-shot IC 3-1 is also set and produces a convert Command pulse at IC 2-6, and Convert Status goes high at IC 4-6. Conversion will be complete well before Transmit Delay has timed out, and Convert Status will go low.
8. Transmit Delay times out at IC 5-1 and goes low. This produces a low transition at Transmit Command IC 2-10, and the sequence continues from Step 6, cycling until the last selected channel is reached.
9. During transmission of the last channel, Last + 1 channel is selected, and at the end of the last transmission the Last + 1 channel is digitized and the system waits for time-out of Transmit Delay. When this goes low, a transmit command is generated, the transmitter fires, the counter is incremented, Last Channel + 1 select goes high, and this positive transition is returned via a programming jumper to the reset of IC 1-12, shutting down system power before the Last + 1 transmission can be accomplished. The system then waits for another positive transition from the clock to initiate the sequence again.

## A.7 Transmitter Specifications

TABLE 2: Transmitter specifications

A parts list for the transmitter is given in Appendix A.1.

Power: 2 air cell batteries at 1000 amp-hrs each  
Current during transmission: 700 Ma at 4.8 volts  
Current during idle: 12 $\mu$ a at 5.2 volts  
Battery life: 3 years at one 2-word transmission per 10 min  
Input signal: -5 v to + 5 v  
Minimum signal input period: 2 hours for 10 min sample rate  
Resolution: 2.5 mv  
Zero shift: 50 mv max  
Quantifying error: 1/2 LSB or 1.25 mv  
Housing: Plastic Skydyne water resistant  
Power input: MS connector (5 pin)  
FSK output: MS connector (2 pin)  
Analog input: "Pressure Relief" connector  
Special input: External clock (wired to 5 pin MS connector)  
Special output: External switched power (wired to 5 pin MS connector)



## B. Digital Receiver

Following the receiver design details given by Allen (1976), the digital receiver decodes and temporarily stores information sent to it via phone line, radio, satellite or other communication link. Up to 16 different data inputs may be decoded by a single receiver. This could be from 16 different transmitters sending one data input each or from one transmitter sending 16 data inputs.\* For the present system each receiver is set to decode one phone line channel only and the transmitter bit rates must all be the same. The stored data is available in latches with BCD format on the back plane of the receiver, either for monitoring or for multiplexing via the interface unit to the digital tape recorder. Channel 1 transmissions are loaded on latch 2 channel 2 on latch 3 and so forth. A bussed data and ID output are available for monitoring data transmissions as they are received. A change of one in the least significant bit corresponds to a 2.5 MV (nominal) change on the input of the particular instrument being monitored. 2048 counts corresponds to 0 volts input to the field transmitter. Full range is  $\pm 5$  v corresponding to zero and 4096 counts. This follows from the 12 bit analog to digital conversions. The relation between input field voltage and counts received is:

$$\text{volts} = \frac{2.45 \times \text{counts}}{1000} - 5.0 \text{ volts}$$

Each channel has an analog output derived solely from the least two significant digits. This output remains at a fixed voltage unless the latch is updated with a new and different transmission. A block diagram of the receiver is shown in Figure 9. Table 3 shows the receiver specifications. The receiver consists of two main sections, the demodulation section and the decode and store section which will now be discussed:

\* continuous transmit mode

TABLE 3: Receiver Specifications

<u>Power Input</u>	<u>Current Drain</u>
+ 15 v	~ 140 ma
- 15 v	~ 31 ma
5 v	~ 1.3 a
Input impedance	10 K
Analog output	0→ 10 volts
Range	-5 to +5 volts
Resolution	~ 2.5 mv (1 count, 1sb)

## B.1 Summing amplifier - filter - FSK Discriminator

### Demodulator section

The incoming FSK signals from as many as 4 different phone lines are demodulated by this card. A summing amplifier allows for connection of several (4) phone lines into a low pass filter (about 800 Hz cut off for channels presently used between 300 and 600 Hz) from which the FSK signal is fed into the input of the discriminator. The block diagram of the section is shown in Figure 10. The detailed circuit diagram is shown in Figure 11 (tuned to 480 Hz). Table 4 contains the general discriminator specifications.

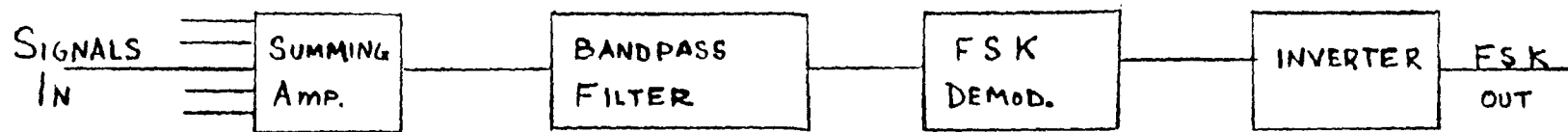


Figure 10: Block Diagram of Demodulator Section.

NOTES: 1. \* INDICATES FREQUENCY DETERMINED COMPONENTS

2. CIRCUIT AS SEEN FROM COMPONENT SIDE OF BOARD (PINOUTS)

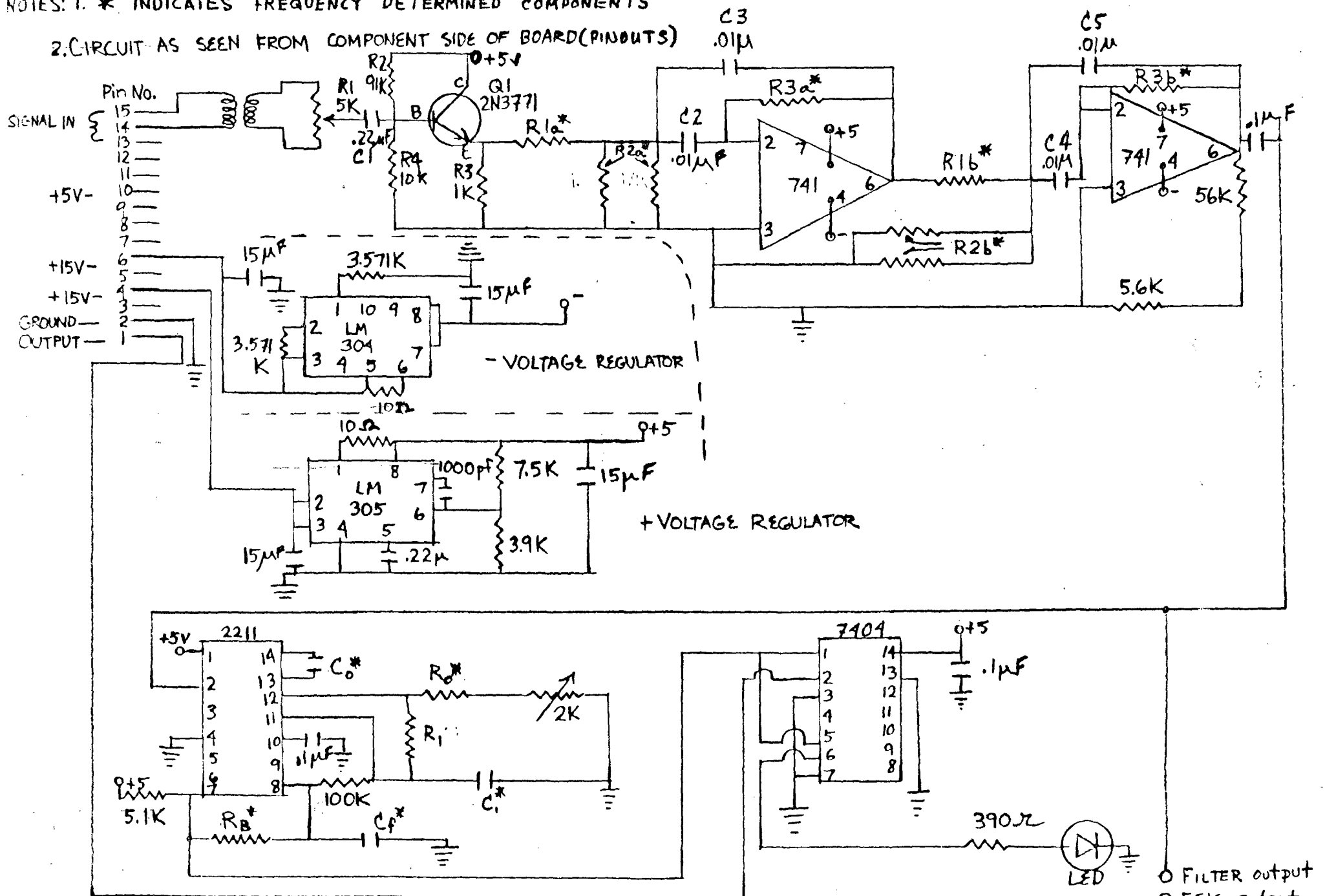


Figure 11: Detailed Circuit Diagram of the FSK Discriminator (tuned to 100 kHz)

The FSK Discriminator takes as an input either of two frequencies (Mark, Space), with the output at TTL Logic levels. It converts pulsed sine waves at the two frequencies to a 0-5 volt pulse train output. The discriminator consists of two regulated voltage supplies for the filter, an input section, a filter section, the 2211 Exar chip as the demodulator and the 7404 inverter and LED driver.

The voltage supplies are provided by a LM305 for +7v and a LM304 for -7v regulated power. The signal from the filter is coupled to the discriminator by means of a transformer. The level potentiometer adjusts the input signal level up to about 1/2 volt peak-to-peak (which may result in signal clipping). The output of the emitter-follower is then fed to the two stage bandpass filter. This bandpass filter and also the low pass input filter uses 741 operational amplifiers to simulate the effects of inductors. This is convenient since inductors in the low frequency range generally are large. The passive equivalent circuit for the bandpass filter is shown in Figure 12. If the input impedance of the second stage is high compared to the output impedance of the first (as is the case for operational amplifier) then transfer function for the filter in terms of its equivalent circuit is:

$$F(s) = \frac{s}{s^2 L_1 C_1 + R_1 C_1 s + 1} \times \frac{s}{s^2 L_2 C_2 + R_2 C_2 s + 1} \cdot K$$

one  two

Each section is a / - pole bandpass, so the combined effect is a / - pole filter, with an attenuation of -12db/octave when the frequency is far enough away from the poles so their effects are not important. Location of the pole of one section close to the lower band edge and the pole

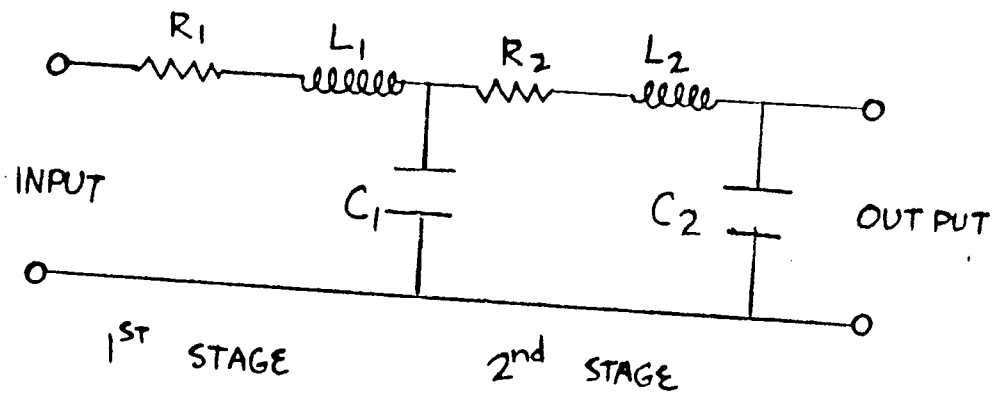


Figure 12: Bandpass Filter Equivalent Circuit.

of the other section close to the upper band edge generates a suitable bandpass response.

The filtered signal is the input to a FSK demodulator chip (EXAR 2211 pin 2). The 2211 uses a first order phase lock loop to convert a frequency to a high or low level. The high frequency input causes a low level out of the chip. This necessitates inverting using a 7404. Another inverter in the 7404 is used to drive an LED with a 400 ohm series resistor to limit LED current. Figure 13 is the circuit diagram for the entire card including low pass filter and summing amplifiers.



TABLE 5: Discriminator Component Values

This table contains approximate values for the components in the filter and FSK sections. Figure 13 is the desired bandpass filter response.

## FILTER SECTION:

FREQUENCY (Hz)	$R_1$	$R_2$	$R_3$
380 $\pm$ 20	39.789 K $\Omega$	1134 $\Omega$	1.591 M $\Omega$
480 $\pm$ 25	39.789 K $\Omega$	703 $\Omega$	1.591 M $\Omega$
595 $\pm$ 30	26.526 K $\Omega$	692 $\Omega$	1.000 M $\Omega$
735 $\pm$ 40	20.0 K $\Omega$	689 $\Omega$	795 K $\Omega$
900 $\pm$ 45	18.0 K $\Omega$	307 $\Omega$	700 K $\Omega$
1360 $\pm$ 45	18.0 K $\Omega$	200 $\Omega$	700 K $\Omega$
1700 $\pm$ 45	18.0 K $\Omega$	130 $\Omega$	700 K $\Omega$
2040 $\pm$ 45	18.0 K $\Omega$	86 $\Omega$	700 K $\Omega$

## FSK Section:

$$R_B = 510 \text{ K}\Omega$$

2K center frequency pot

Supply voltage 5 v  $\pm$  5%

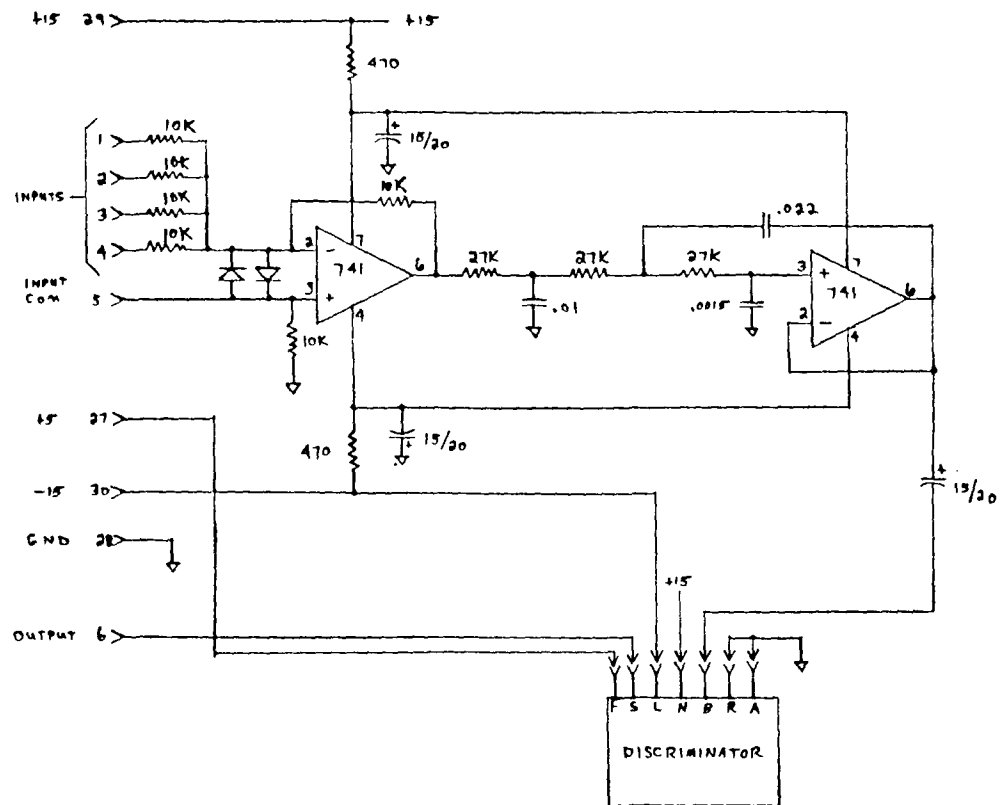


Figure 13: FSK - Summing Amplifier Card. (After R. Allen)

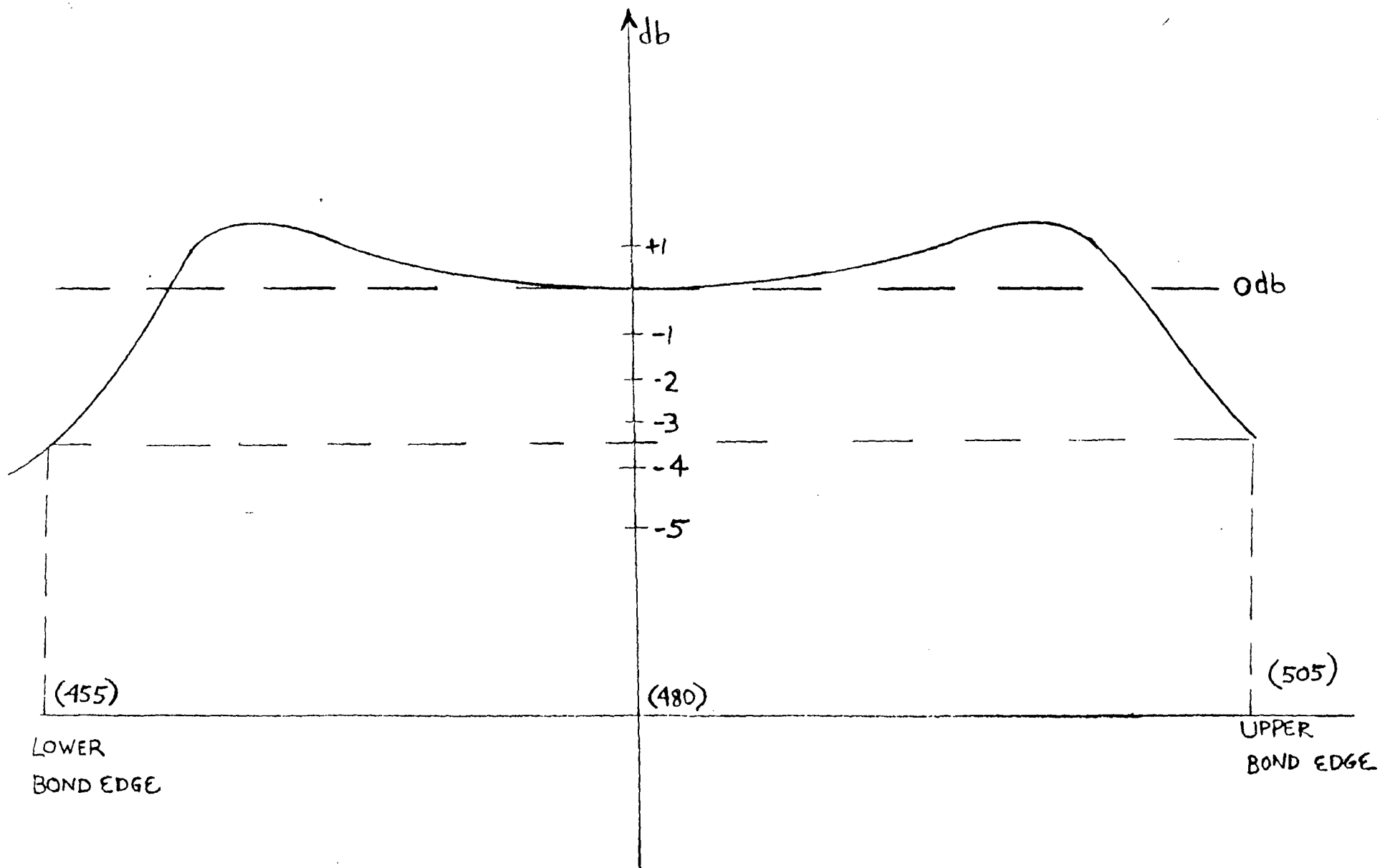


Figure 14: Bandpass Filter Response for the FSK Discriminator.

### Detailed Tuning Procedure Steps

After assembling the circuit according to Figure 11, the two stage bandpass filter must be correctly tuned for the desired frequency band with the peak filter response at the average "center frequency" of the two FSK tones. The detailed steps are listed below.

Since each 741 stage has frequency determining components  $R_1$ ,  $R_2$ ,  $R_3$

- 1) Install appropriate value for  $R_1$  and  $R_3$  from Table 5 at first 741 stage.
- 2) Repeat step 1 for second 741 stage.
- 3)  $R_2$  will be the frequency determining component which will set the -3 db points for the upper and lower band edge.
- 4) Install in both 741 stages the  $R_2$  values from Table 5 corresponding to the center frequency selected. Attach decade resistance boxes in parallel with both  $R_2$  resistors.
- 6) Sweep through the frequency spectrum while monitoring the output to check to see that the filter response is approximately correct. The peaks should be no more than 100-200 Hz from the correct values.
- 7) With the parallel decade boxes in both stages, adjust the first stage box so that the lower band edge signal level (decibel) is down 3 to 5 db /from the zero db level which is set at the center frequency. On the sweep to the upper band edge check and reset the center frequency db level to zero if necessary. Do this for every sweep from lower to upper or vice versa. At the upper bandpass edge adjust the second box for -3 to -5 db also. Go back and forth to get the desired result.
- 8) Replace the decade resistors with carbon quarter watt, 5% resistors.

If the above procedure does not work fairly quickly it will probably be necessary to reset the  $R_2$  values to more closely approximate their final value. Also, when selecting the carbon resistors measure the required resistance with a Digital multimeter, then select a carbon resistor a few ohms below this value. Soldering will bring it to the right value.

After the filter is properly tuned, the FSK chip must be tuned to the same center frequency. To achieve this replace  $R_o$  in Figure 11 with a decade resistance box and monitor the output of the VCO in the phase lock loop (PLL), pin 3, with no input and pin 2 shorted to pin 10. Adjust the decade box so that the VCO free-running frequency is the desired center frequency. This value of  $R_o$  should be  $\sqrt{\frac{30 \text{ K}\Omega + 10 \text{ K}\Omega}{}}$  to give the best temperature characteristics. It may be necessary to change  $C_o$  to get this desired value.

Once the VCO frequency is set it will still be necessary to fine tune the PLL using the potentiometer.

TABLE 6: Definitions and Formulas

Table 6 contains some definitions and formulas which may prove useful for optimum component selections.

<u>Component/Variable</u>	<u>Definition or Function</u>
$f_l$	low frequency
$f_h$	high frequency
$f_o$	"center" frequency, $(f_l+f_h)/2$
$R_o$	determines $f_o$ . Choose $\approx 30 \text{ K}\Omega$
$C_o$	determines $f_o$ . Choose polycarbonate capacitor. $f_o = 1/R_o C_o$
$f_{oh}$	highest frequency which PLL will lock onto
$f_{ol}$	lowest frequency which PLL will lock onto
$R_1$	Controls track range. Adjust $R_1$ so $f_{oh} > f_h$ and $f_l > f_{ol}$ . $R_1 = R_D \cdot \frac{f_o}{f_l - f_h}$
$C_1$	sets loop damping. increasing $C_1$ improves noise rejection, but slows PLL capture time. $C_1 = 0.25 C_o$
$C_f$	Data filter capacitor, 3/bit rate, microfarads

Generally the PLL bandwidth should be 10-20 Hz greater than the signal bandwidth. The dead-band (dead band or hysteresis is a characteristic of the EXAR 2211) should be 6-12 Hz.

A component location diagram for the discriminator is in Appendix B-1.

## B.2 Decode, convert and store section.

This section consists of 3 basic parts: A decoder (Larse REDE unit) which decodes incoming serial data trains, the binary to BCD convert logic and an addressing chip to load the data into the correct latch. Figure 15 is a detailed circuit diagram.

The data from the discriminator flows to the input of the REDE unit which converts the serial data train to a parallel format provided the internal data checks are passed. The parallel binary data words are converted to BCD and the ID information (part of every transmission) is used to load the BCD data into the appropriate latch. What follows is a more detailed description of each of these 3 parts.

### Binary - BCD Conversion

The Larse "REDE" output contains 4 bits of identification data (0 - F in Hexadecimal) and 12 bits of binary data. Since all recording is done in BCD it is necessary to convert this binary number to BCD. The EOW\* (end of word) pulse is used to start this conversion. EOW pulse does the following:

- A. Loads 12 binary data bits into binary down counters (IC - 1, 2, 3)
  - B. Clears the BCD up counters (IC - 7, 8, 9, 10)
  - C. Toggles open the count gate at IC 4- 5 (See clock operation below)
- IC 4-6 goes high enabling the count clock whose output (IC 4-8) is led to the clock inputs of the two counter strings, one counting down in binary from the loaded value, the other counting up in BCD from the reset zero.

The up counter works as follows: Each clock pulse causes IC3 to count down one count. When the value of this counter reaches zero a borrow pulse reduces the counts preset in IC-2 by one. Eventually all

\* strobes low when a transmission has passed security



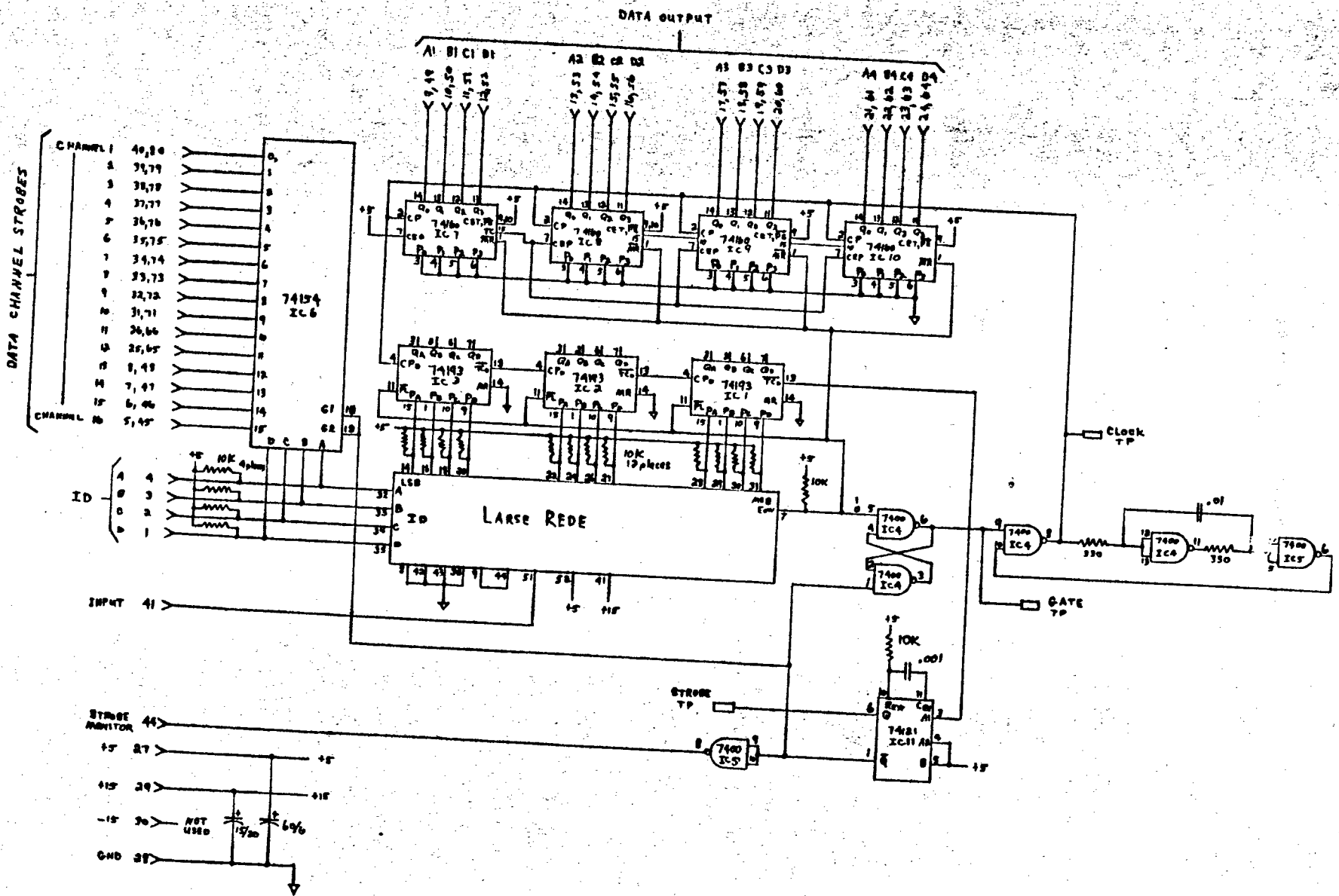


Figure 15: Circuit Diagram of the Decode Convert and Store Section. (After R. Allen)

counters reach zero at which time the borrow pulse from IC 1-13, stops the clock. During the down counting the number of pulses is counted up on the BCD string as follows: The clock is fed to all stages of the BCD counters, but "Enable T" (pin 10, IC 9,10) prevents counting except when "Carry" (pin 15) goes high. For example when IC -7 goes from 9 to 0 a carry pulse is fed to pin 7 of IC - 8, 9 and 10. Since counting can occur only when both enables are high, only IC - 8 increases by one count. When IC - 8 goes from 9 to 0 IC - 9 gets a carry pulse in addition to an enable pulse while IC - 10 only gets one enable pulse. Since two simultaneous pulses are necessary, only IC - 9 advances by one count. IC - 10, the most significant digit, advances when it receives carry pulses from IC - 9. Counting up stops when the clock is shut off.

#### Clock Operation

IC 4- 6 controls the clock. When EOW strobes low the clock is enabled and produces a pulse train of fixed frequency until the "end of count" at IC 11-1 strobes low. This causes IC 4 - 6 to go low (EOW has already gone high) and the clock is shut off until the next EOW strobe.

#### Addressing

The LARSE card has a 74154, a 16-bit decoder and addressing chip, IC 6. After BCD conversion is complete, a pulse appears at IC 6-18, 19 which causes the data on the bus to be loaded in the correct latches. The particular latch selected depends on the ID present at IC6 - 20, 21, 22, 23. Since there are 4 bits, 16 possible outputs are possible, one for each input channel. ID n causes the data to be loaded in latch n + 1. For example the data from ID 7 is loaded in latch 8.

### The LARSE REDE

The LARSE SEN unit transmits a serial code. Each transmission consists of 2 code words which contain identical information (including 16 bits of data and ID) A word is 34 bits, each with 8 elements. Each element contains 2 data bits and 2 clock bits. In order for a transmission to be accepted (EOW to strobe low) the two transmitted words must be identical in every bit. In addition to <sup>this</sup> security test being passed the LARSE REDE operates synchronously with the LARSE SEN in such a way that the REDE samples this incoming data train in the center of each bit to determine its status, either low or high.

A transmission is accepted when the following tests are passed:

#### Code element tests

- o The REDE unit checks that no more than two negative transitions occur per code element.
- o All clock bits must be in their proper position, of proper polarity and of proper length.
- o Data bits must be in their proper position
- o Elements cannot have too many or too few transitions.

#### Code word tests

- o Each word must contain eight code elements.
- o Each word must be preceded and followed by word or frame (one or more words) synchronization bits.

Reception can be made easier (but more error prone) by rewiring the REDE so each word is considered independently. In this case a transmission is accepted if either of the transmitted words passes its tests.

### Latch - Digital Analog Conversion

Each card contains 4 "Latches" (93L08) and two Zeltex D/A (Digital to Analog) converters. The last transmission (bussed data) is present at

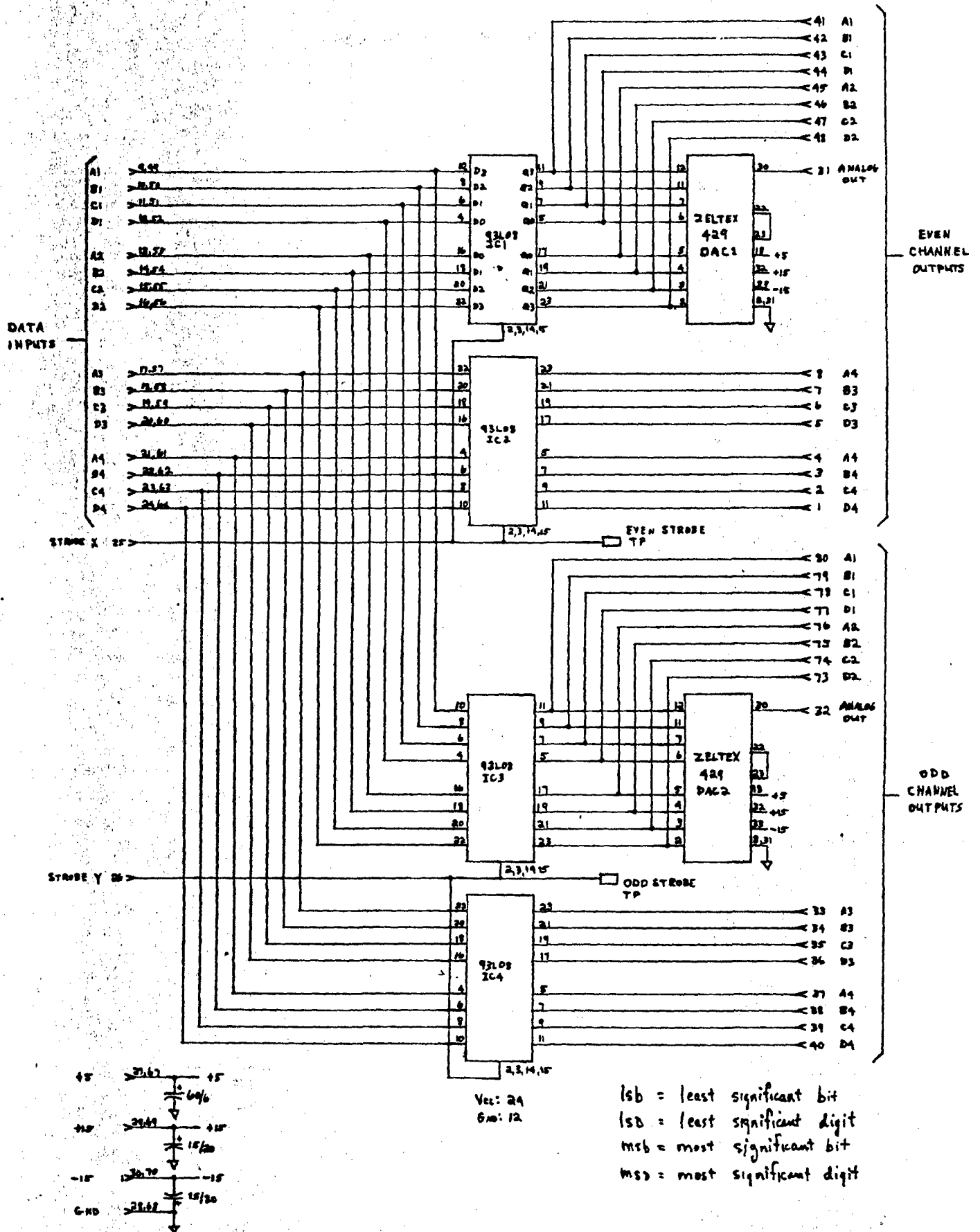
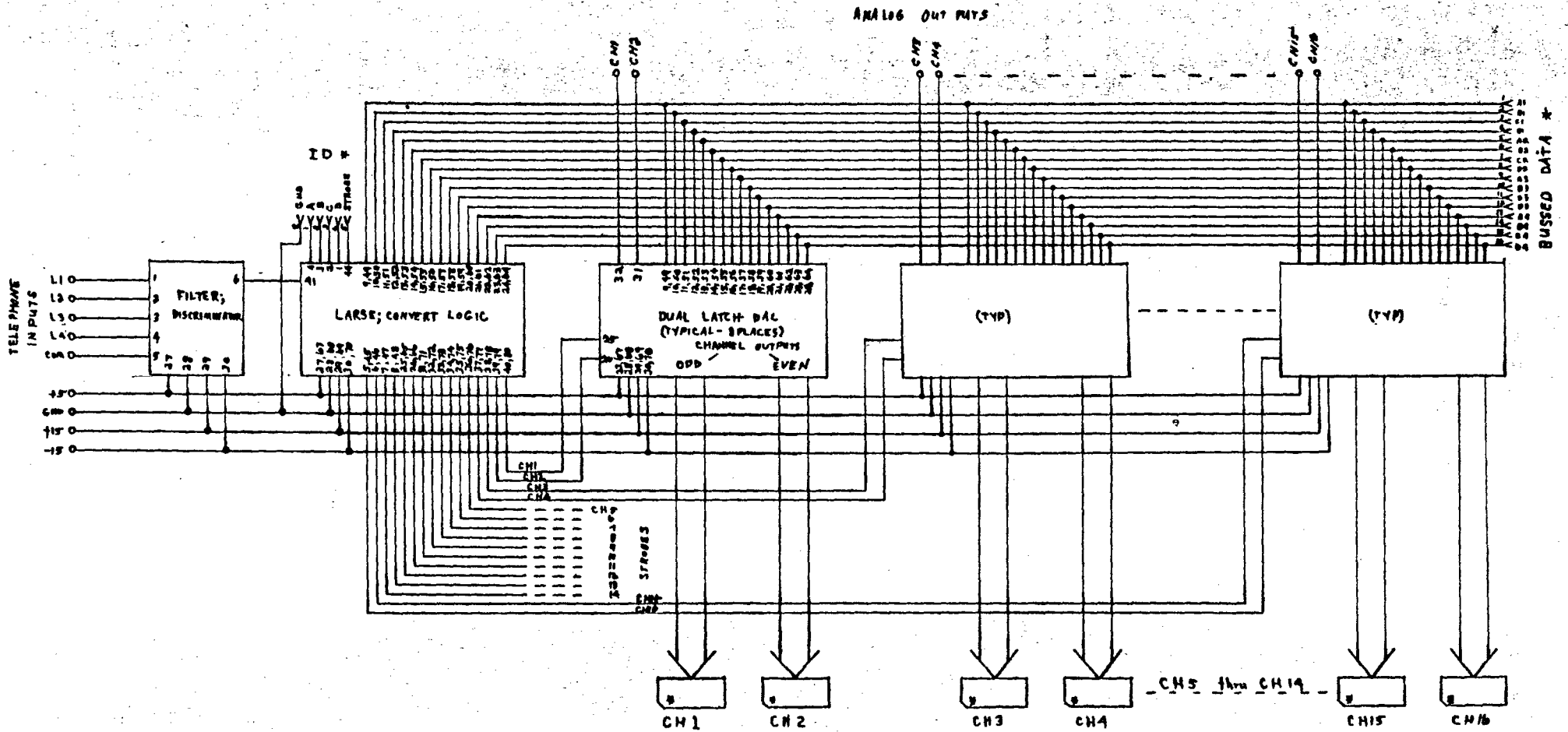


Figure 16a: Circuit Diagram for Receiver Dual Digital-to-Analog Converter and Data Latch. (After R. Allen)



NOTE: DATA CHANNEL OUTPUT SOCKET CONNECTIONS SAME AS BUSSED DATA OUTPUT SOCKET  
 \* 16 PIN DUAL IN-LINE IC SOCKET

Figure 16b: Circuit Diagram for Receiver Mother Board. (After R. Allen)

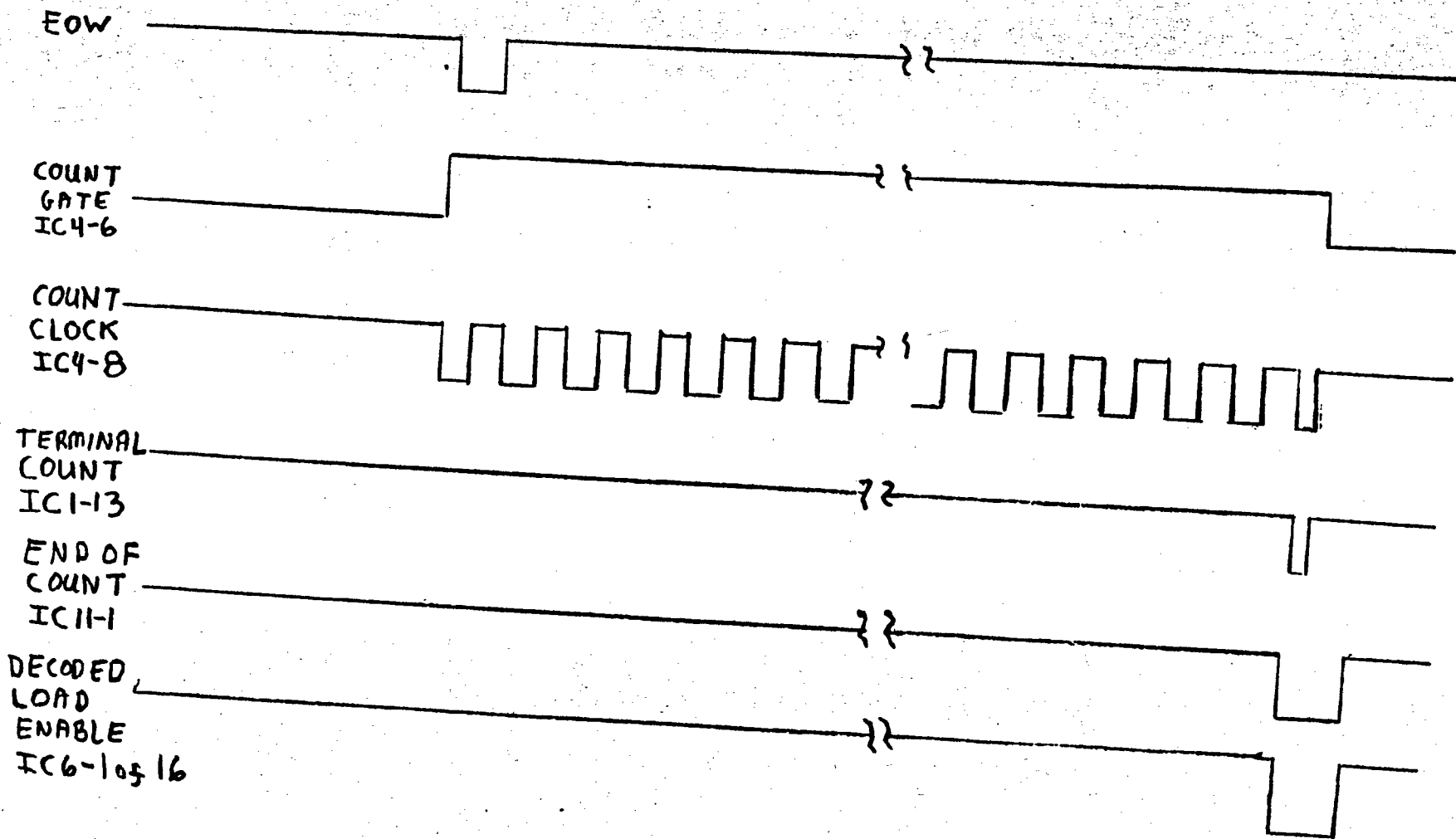


Figure 16c: Receiver timing diagram. (After R. Allen)

the inputs of the latches. The appropriate latch receives a load strobe from the 74154 and the new data appears at the latch outputs.\* The 2 least significant digits are returned to analog by a 2 digit ZD-429 DAC. Its output is 0-10 volts, each count on the least significant digit being 0.1 volts and on the more significant digit, 1.0 volts. Thus, the digital number  $2068_{10}$  will produce an output of 6.8 volts. This voltage is used for analog chart recording. See Figure 16a for the circuit diagram. The wiring of the mother board is shown in Figure 16b and an overall timing diagram for the receiver is shown in Figure 16c. A parts list for the receiver is given in Appendix A-2.

\* Note: if no transmissions for a particular latch are received, the data present on the latch outputs can be arbitrarily old.

## C. Interface and Cascade Time Expander

### C.1 Digital interface unit

The interface controls a 7-track IBM computer compatible tape recorder and performs the function of dumping 116 parallel 4 bit BCD characters sequentially and as a single word on this recorder. The information contains identification data, master clock time, data and error code. Each record consists of a 2-digit instrument identification, a 4-digit data sample and an error code from each of the 15 instruments, universal time and the 2 digit interface identification. The interface also provides the necessary logic pulses for proper tape operation including zero conversion (to binary 1010). Each time 4 parallel bits (a BCD character) is presented at the data output a "write pulse" (WP) is generated. This pulse causes a tape advance of  $1/556$  inch and the 4 bits are recorded. At the end of the record the interface advances the tape  $3/4$  inch by generation of an "interrecord gap" (IRG) pulse. The operation of recording the 116 characters (1 record) is called a dump and is initiated by a dump pulse. The dump and IRG take approximately 2 seconds for the present system. Dumping at rates of up to four times faster is possible by increasing the MUX clock frequency. Table 7 lists the interface specifications.



**TABLE 7: Interface Specifications and Requirements**

**Power:** 1 amp at 5v

**MUX Clock:** 100 Hz

**Data Capacity:** Fifteen 16 bit BCD words plus a 9-digit time code

**Tape Recorder:** See Cipher Section

**Dumping more than one interface:** See Cascade Section

**Maximum Dump rate:** 300 bits/second

**Logic levels:** All 5 volt TTL

**Zero conversion:** To binary 1010

The interface consists of 15 data cards, a sequencer card and 2 "data time code boards" one of which has solely a time gating function.

The order of dumping is:

Interface ID (tens)

Interface ID (units)

Time (100's days 2)

Time (100's days 1)

.

Time (1's of seconds 1)

First Data card ID (tens)

First Data card ID (units)

First Data (thousands)

First Data (hundreds)

First Data (tens)

First Data (units)

.

Second Data Card ID (tens)

.

.

Last Data card ID (tens)

.

.

Last Data (units)

The function of each card is detailed below. See Figure 17 for a block diagram of the interface.

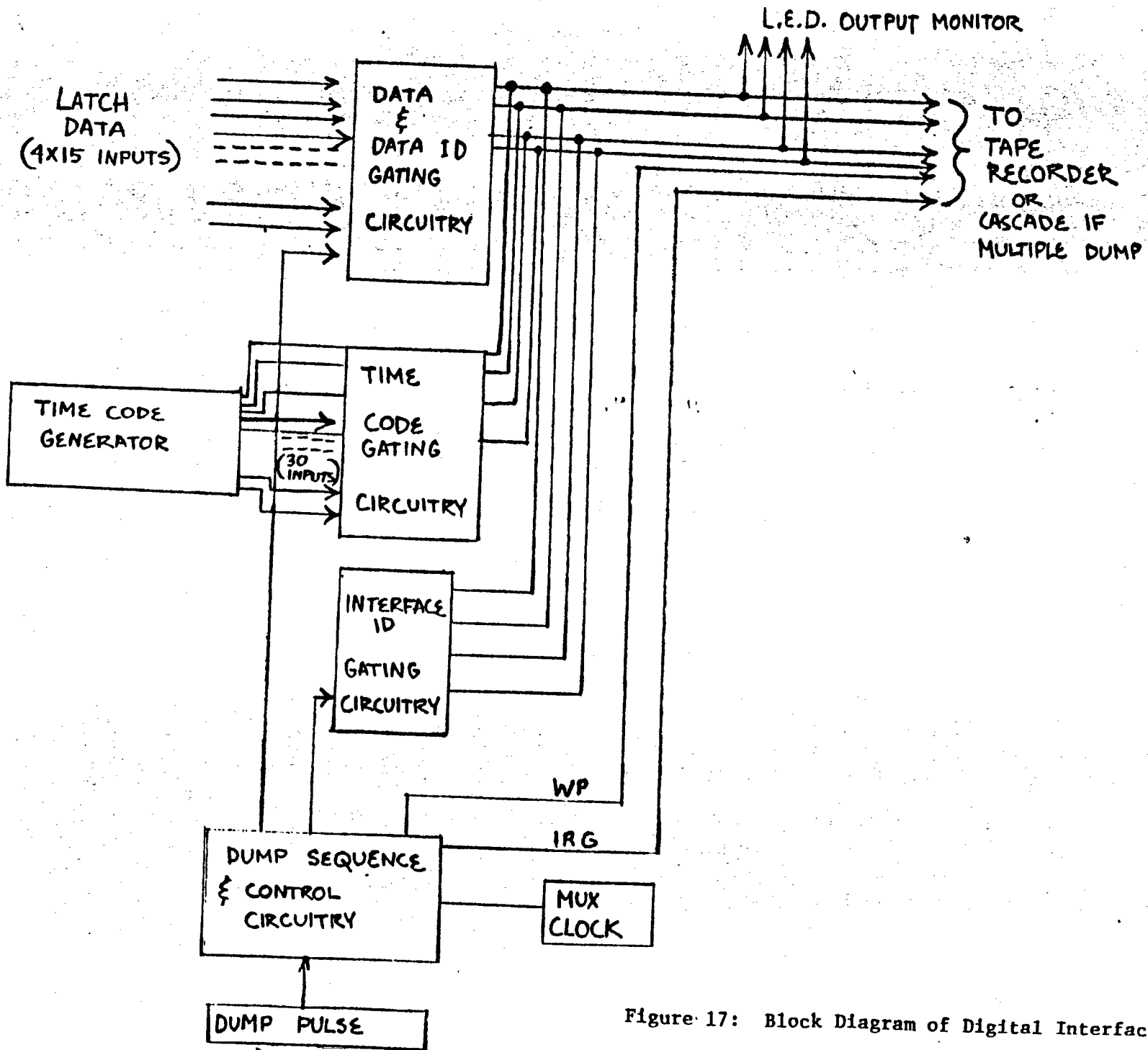


Figure 17: Block Diagram of Digital Interface..

### Sequencer (A18)

The sequencer card controls timing, tape recorder operation, and multiplexing for each data dump. Figure 18 is a detailed circuit diagram. A dump is initiated by the dump control. After the last dump the status of the flip-flop (74107) is cleared (low). The first clock pulse causes "Q" to go high and stay high until it receives the "clear" pulse at the end of the dump. The Q output of the other flip-flop (the DM 74107 is a dual JK) will also go high at the next high from the monostable multivibrator (IC-E4A). This opens the NAND gate output (IC-D3) to the input from the MUX clock. This clock is first fed into a pulse stretcher consisting of 2 sections of a 74123. The output of each stage is inverted, however, so the first stage has the effect of stretching the low portion of the clock pulse train by 87  $\mu$ sec. The second stage then has the effect of inverting the low to a high and subtracting 32  $\mu$ sec from the 87  $\mu$ sec. The result is that the output to the 7400 NAND gate (ICD3-1) has its high portion stretched by about 50  $\mu$ sec. The write pulse uses the identical scheme to stretch the pulse train an additional 50  $\mu$ sec.

The pulse train from IC-D3-3 is fed to a 4-bit binary counter. Each pulse to the counter input (IC-C1-14) produces a pulse on the output of IC-B1 which is used to gate the interface ID and then time onto the data bus. The 50  $\mu$ sec delay in the write pulse insures that the data will be present when the write pulse goes high. When the last time data has been gated a pulse from IC-B1-14 causes IC-D4-8 to go high which resets IC-C1 to the zero state. This opens the NAND gate IC-D3 which feeds the clock pulse train into another binary counter (IC-C3). As soon as the first clock pulse has past, IC-B3-1 goes high which disables the second 74154 (IC-B1-18, 19). This prevents dumping of time or interface ID data at the same time data is being dumped. When a pulse appears on IC-B3-17 (the pulse for the last card) the monostable multivibrator IC-E2 is triggered. This provides the Interrecord gap to the Cipher (the Q output, IC-E2) and a reset pulse to the dump control input (IC-D2) which in turn closes the MUX clock input gate IC-D3. This prevents any further cycling in either IC-B1 or IC-B3. The interface is now ready for the next "dump" pulse.

#### Data Cards (A1-A15)

The interface contains 15 data cards (see Figure 19) each with a 2 digit "ID", a 1 digit error flag, and 4 data digits. The function performed by this card is to gate the data present at the inputs onto the multiplexed data bus. This is done using a 7442 decoder. When input 12 of the 7442 goes low (data card select pulse) the outputs are enabled and pulses sequentially appear on outputs 0 to 7 as the BCD input goes from 0 to 7 (pins 15, 14, 13). The low strobe outputs are inverted by a hex inverter (7404) and one transistor. When the "0" output of the 7442

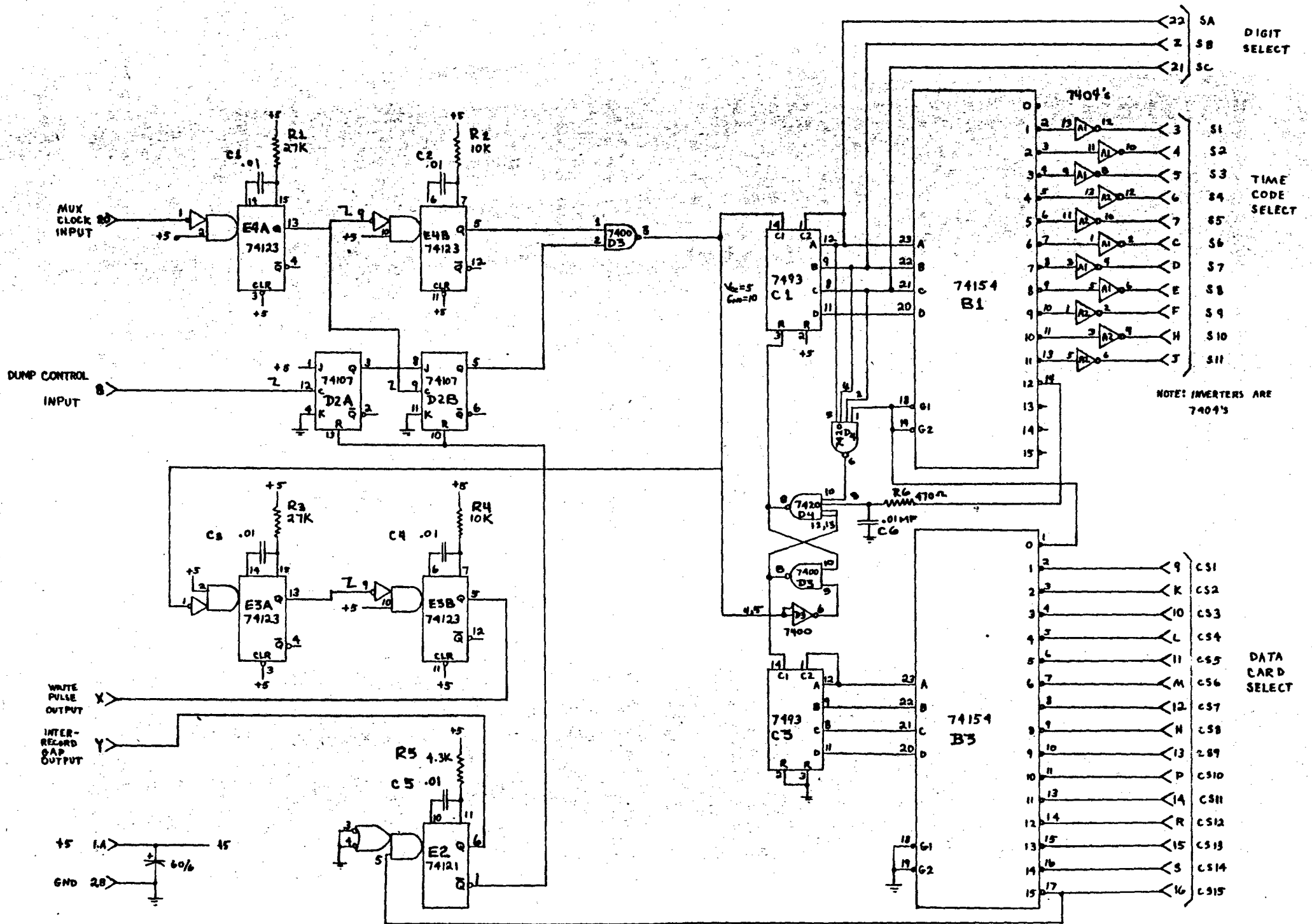
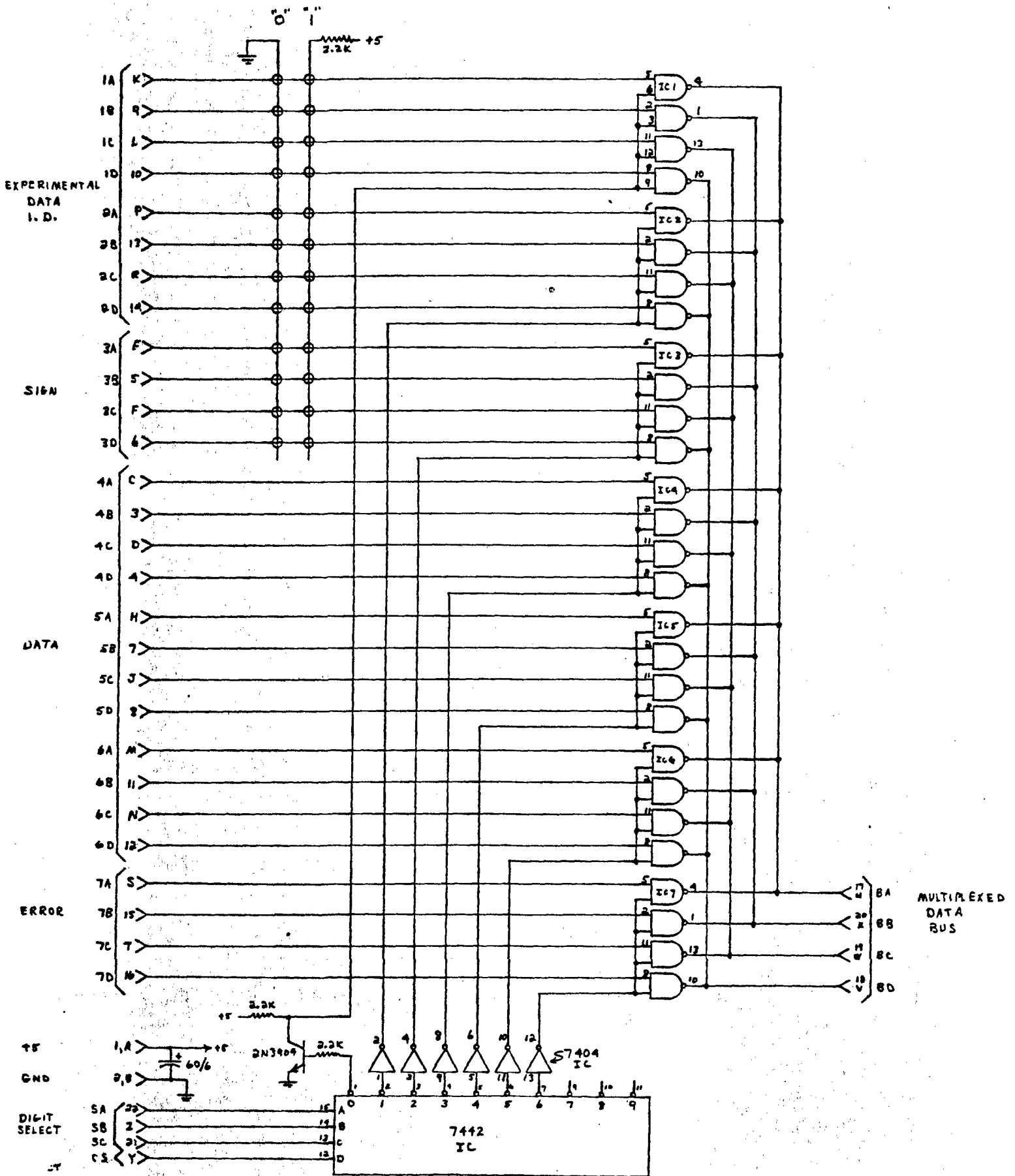


Figure 18: Sequencer Card Circuit Diagram.



NOTE: 1: ALL 2-INPUT NAND GATES ARE 7401'S  
 2: ALL INVERTERS ARE 7404'S

Figure 19: Data Card Circuit Diagram.

strokes low the transistor is turned off and the collector goes high. This enables the NAND gate such that the first digit is gated onto the data output bus. This digit is the tens digit of the data ID. The next pulse gates in the units digit of the ID and soon until the last data is gated through.

#### Time of Day (A16)

The time of day (see Figure 20) gates time information (seconds, minutes and hours) on the data lines. Its operation is similar to the data card except the gating strobes come directly from IC-B1 of the sequencer card.

#### Day Time (A17)

The Day Time board A17 (see Figure 21) performs 4 functions:

1. gates time information on data bus or lines
2. gates interface ID on data bus
3. provides a visual output monitor of the data bus
4. provides zero conversion for all data.

As described for the Time-of-Day card the final gating of time information (days) is completed on this board. As each data (either time identification or input data) are gated onto the data lines four LED's provide a means of visual monitoring. This is particularly useful for initial checking by running the MUX clock at a very low frequency so each data bit can be checked. These LED's are driven by a high current driver (7417). The interface ID is hard-wired to IC-C1 and IC-C2. IC-C1 is the 10's digit and IC-C2, / the units. Giving each interface an ID number is necessary if more than one interface is dumped on a single tape. An overall timing diagram is shown in Figure 22. Figure 23 shows the test point locations. Zero conversion is accomplished with dual 4-input NAND gate (7420). A zero data input is converted to binary 1010. A parts list for the interface is given



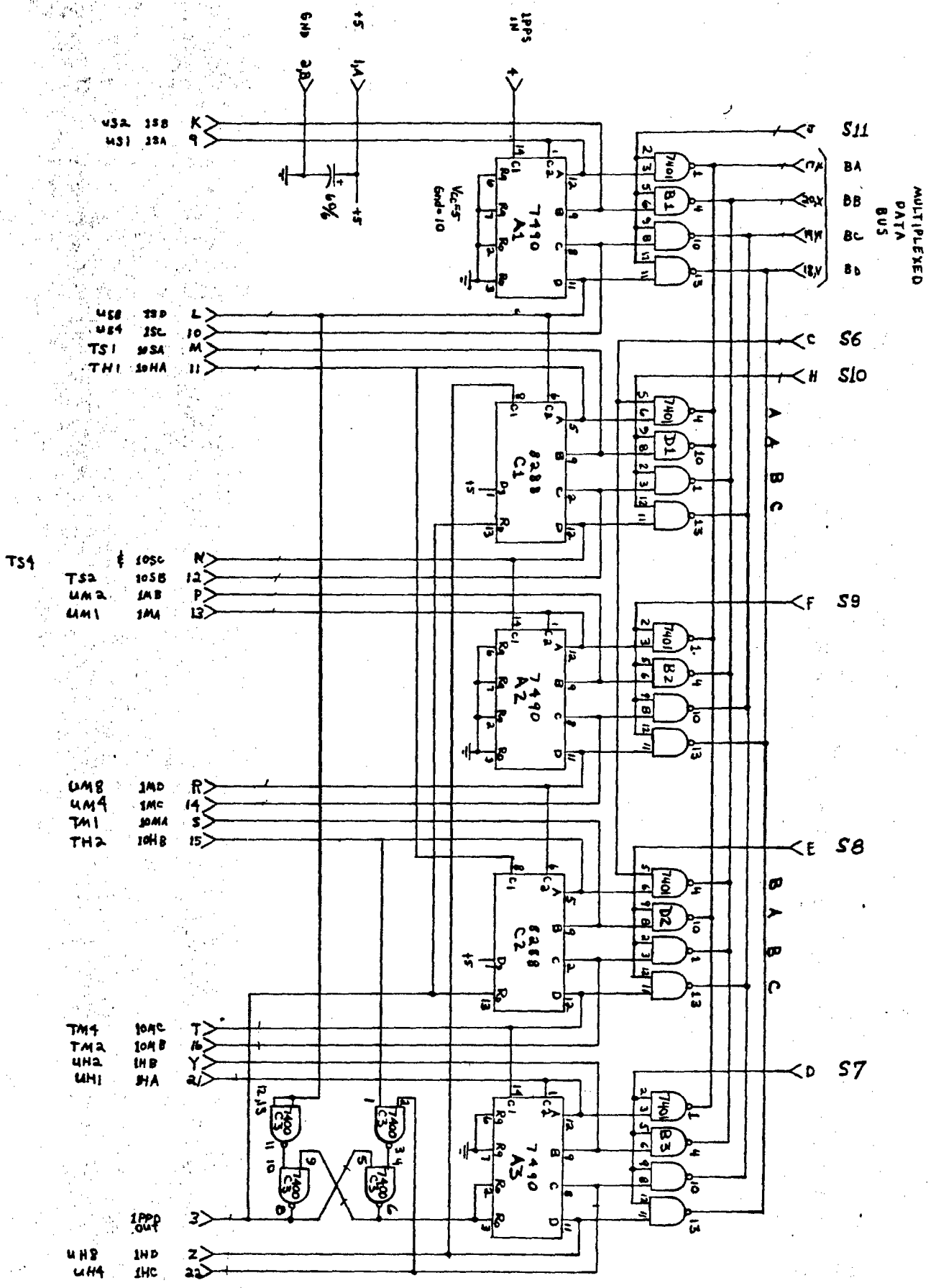


Figure 20: Time-of-Day Card Circuit Diagram.

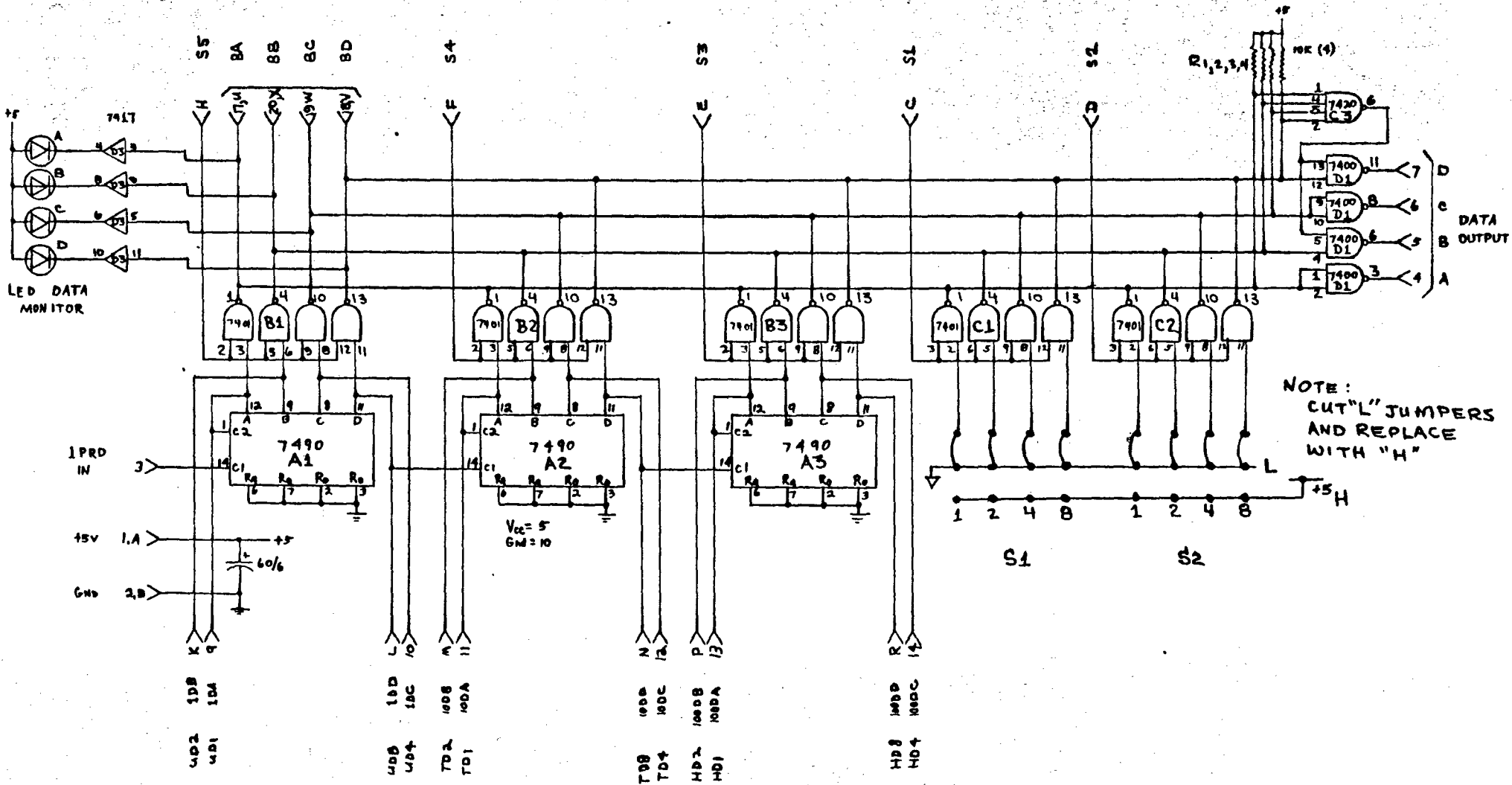


Figure 21: Day Time Code Circuit Diagram.

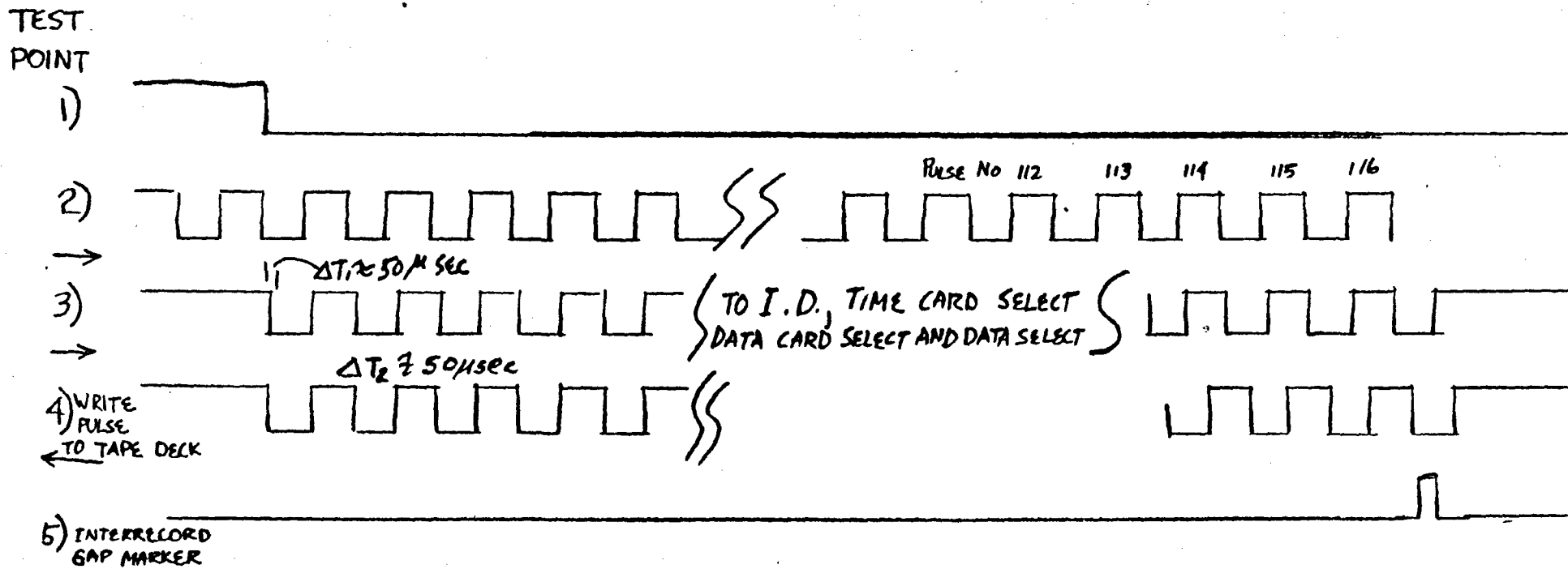


Figure 22: Timing Diagram Digital Interface Sequencer Card.



in Appendix A.3

### C. 2 Cascade time expander

The function of the Cascade-time expander is to allow for dumping of up to 10 interfaces into a single Cipher tape recorder and also to provide enough time code outputs for each of the interfaces. With the present system each interface is given 5 seconds to dump onto the tape. The time expander is necessary for two reasons:

1. As a buffer between the master clock and the digital telemetry system.
2. To provide the necessary master clock fan-out for multiple system operation.

### Cascade Card

The cascade (see Figure 24a) sequences the various interfaces and their inherent tape recorder control logic to a single tape recorder. For the present system it sends out dump pulses to each of the interfaces once every ten minutes. At dump time (determined by decoding time from the master clock) (See Appendix C) a 4 bit binary counter (7493) is enabled and counts at five second intervals. The BCD to decimal decoder (7442) begins by putting out a low pulse on line "zero" (pin 1). This allows interface #1 to be dumped. See Figure 24b for the pulse train at IC3-3. A 7417 driver is used with 10 LED's to provide a visual indication of the dumping operation. A component location diagram is given in Appendix B.3, and the back panel in Appendix D.

### Gate Card

Each interface output (4 bits of parallel data and control functions) is gated to the Cipher digital tape recorder on a common data bus using 7401 NAND gates with the Cascade "dump" pulse or trigger serving as the gating signal as shown in Figures 24c and d. A component location diagram is given in Appendix B.4.

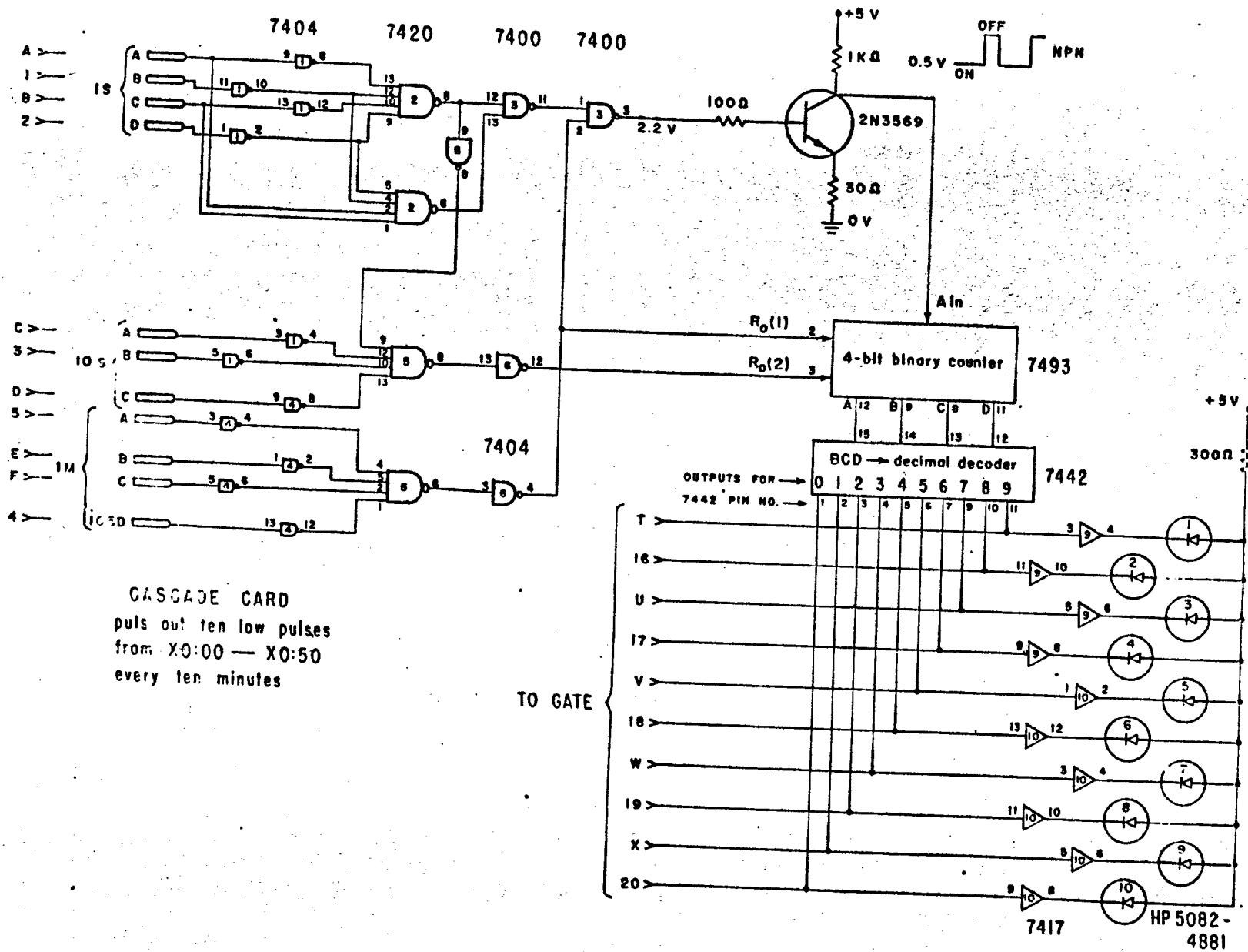


Figure 24a: Circuit diagram for cascade gating control

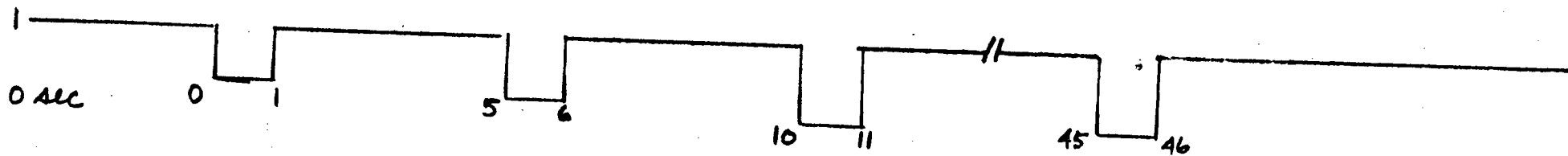
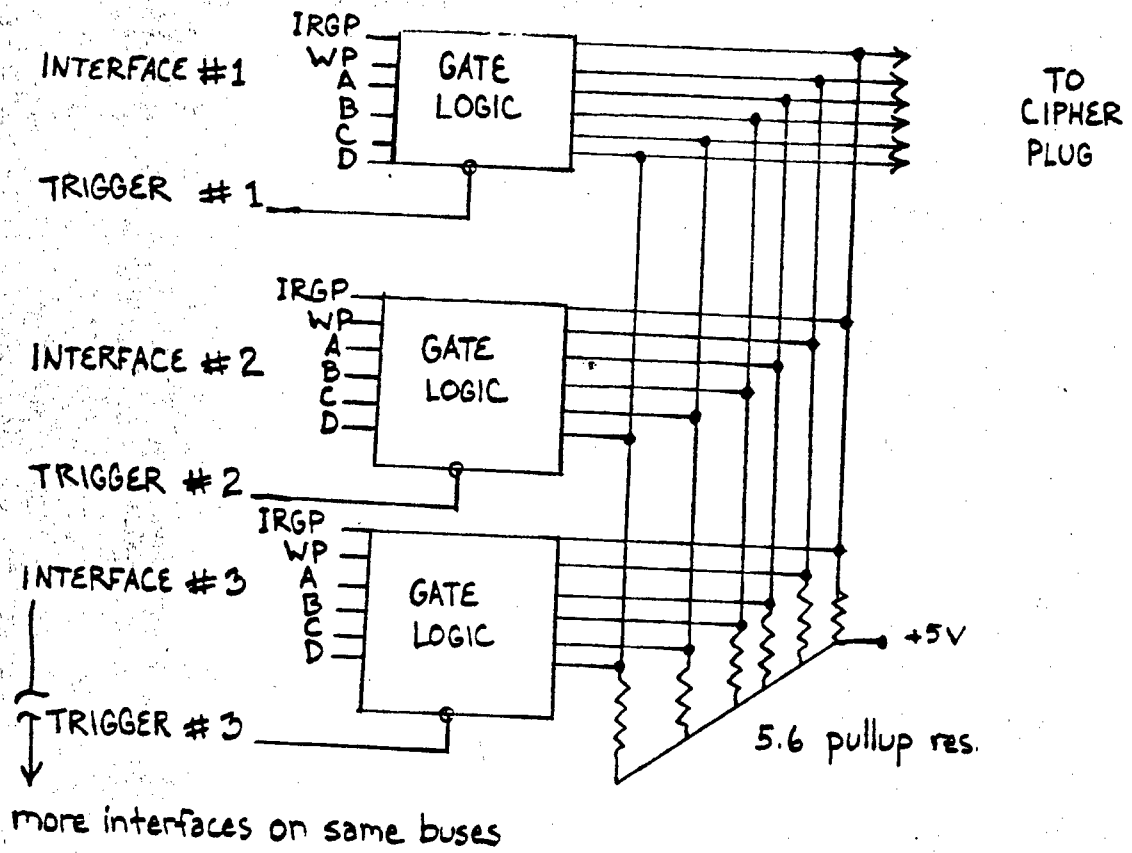
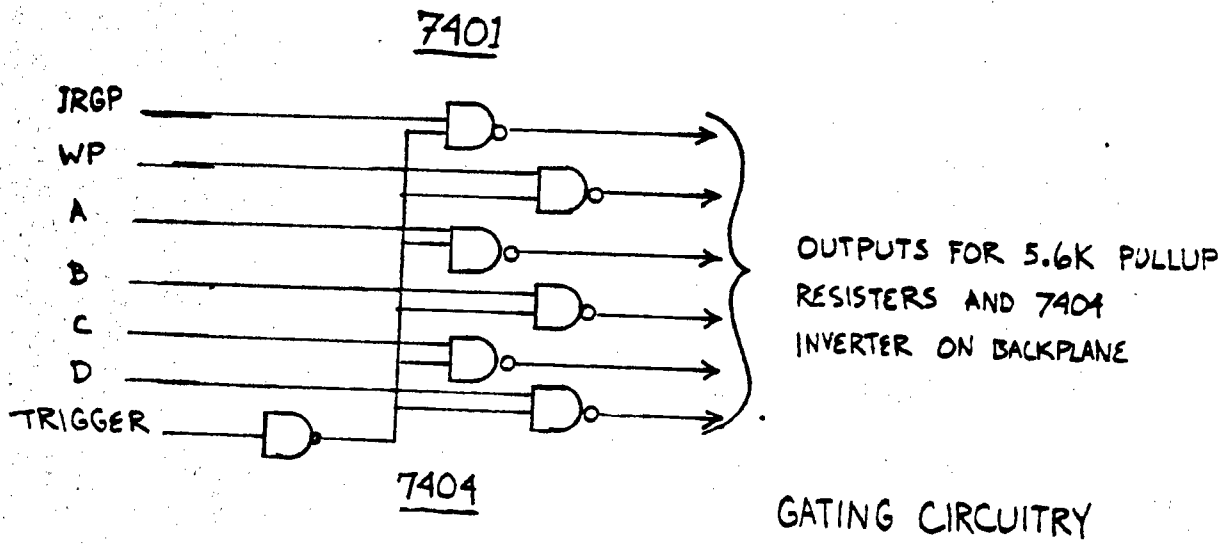


Figure 24b: Cascade Timing Diagram.



GATE LOGIC



GATING CIRCUITRY

Figure 24c: Gate Logic Circuit Diagram.



# GATE CARD AND BACKPLANE

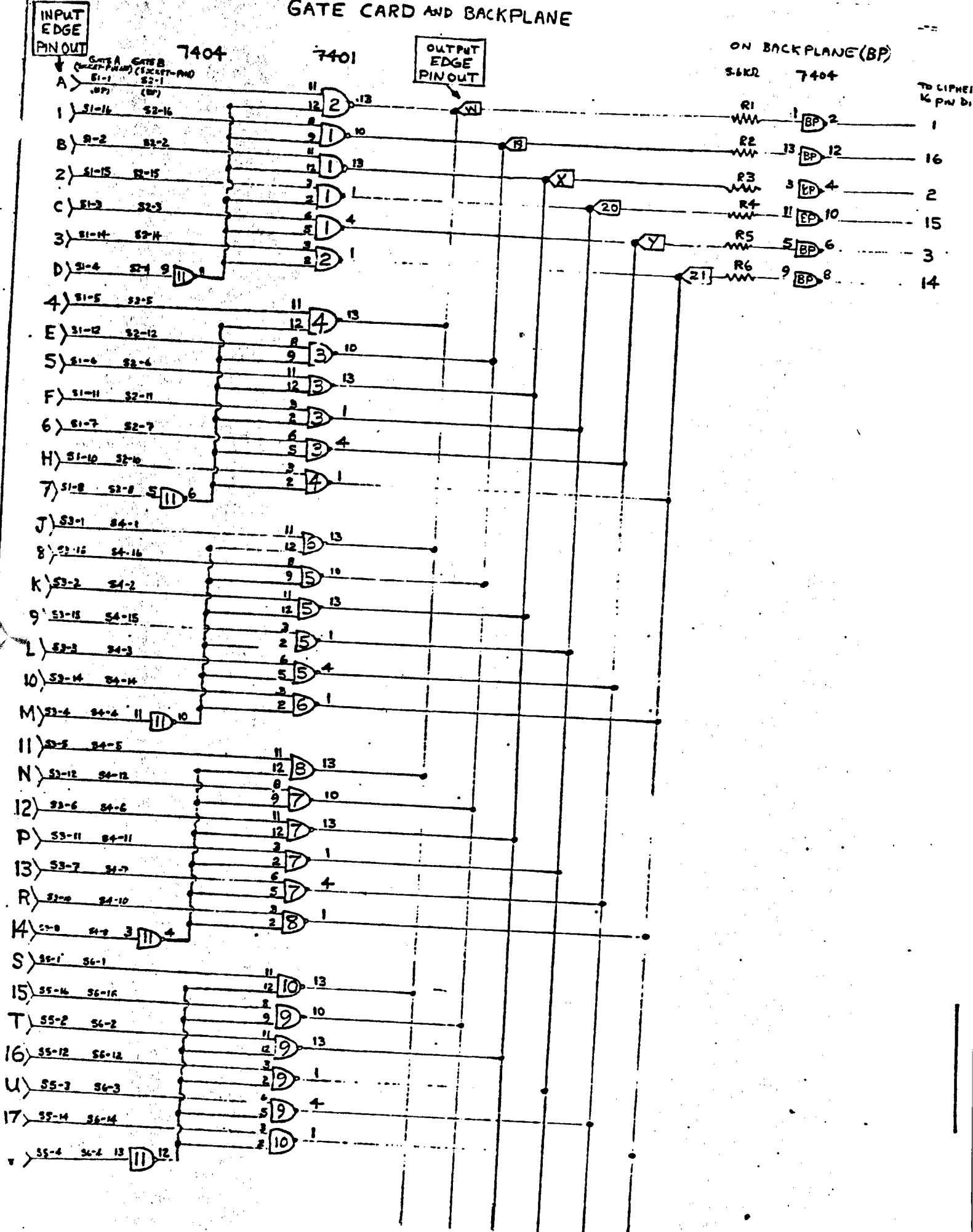


Figure 24d: Gate card and back plane



S = SECONDS

M = MINUTES

H = HOURS

D = DAYS

WIRING FOR (AMPHENOL 133, 143 SERIES)

A 1 SECOND 1

B 2

C 3

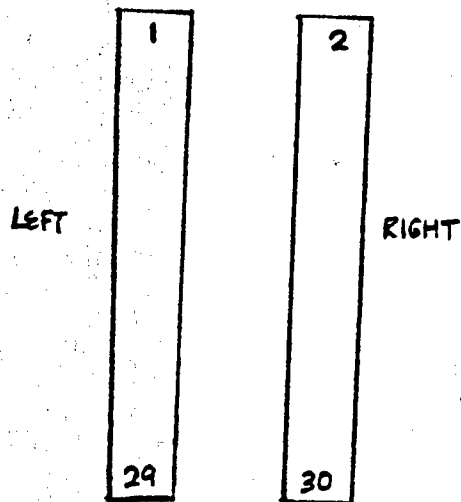
D 4

A 10 SEC. 5

B 6

C 7

THE TIME Input Connection



1SA	1SB
1SC	1SD
10SA	10SB
10SC	1MA
1MB	1MC
1MD	1MA
10MB	10MC
1HA	1HB
1HC	1HD
10HA	10HB
1DA	1DB
1DC	1DD
10DA	1DE
10DC	10D
100DA	100DB
NC	NC

BOTTOM

Figure 25 (cont'd): Time Expander.

### Expander Boards

13 parallel BCD time outputs are provided by the expander boards. The buffer used is a 7404 NAND gate.

The pin outs for the time are shown in Figure 25. All unused inputs should be wired to ground. i.e., 100DC, 100DD.

The wiring for the interface data cable is shown in Figure 26. The lower 8 pins of the bottom two 16 pin DIPS are not connected. Any unused outputs should be wired to ground (dump or trigger excepted) or the Cipher will not operate properly. A parts list for the Cascade is given in Appendix A.4, and a parts location diagram for the expander boards is given in Appendix B.5.

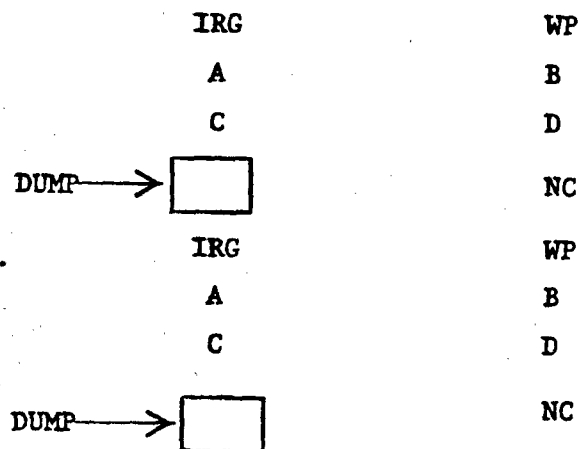


Figure 26: Wiring for interface data cable

#### D. Cipher Digital Tape Recorder

The Cipher digital tape recorder is the last stage of the digital telemetry system. Its function is to record the data present on the interfaces. Each time an interface is <sup>dumping</sup> data simultaneous write <sup>pulses</sup> / occur which causes the recorder to advance in increments as the data are dumped. Each BCD character is accompanied by a write pulse. After the dump is finished an IRG pulse advances the tape about 3/4". At this time the recorder is ready for the next dump.

Since the cipher is designed for 6 channels and BCD uses only 4 the data channels A and B (pin 10, 11 on data plug) are wired to common. The cipher plug must be connected whenever power is on or the tape will advance continuously.

Figure 27 shows the wiring for the cipher plug. The tape recorder <sup>the</sup> specifications are listed in Table 9. The most common characters/tape recorder generate for all possible inputs are summarised in Table 8.

The layout diagram of the complete system without the Cipher recorder is given in Appendix E.

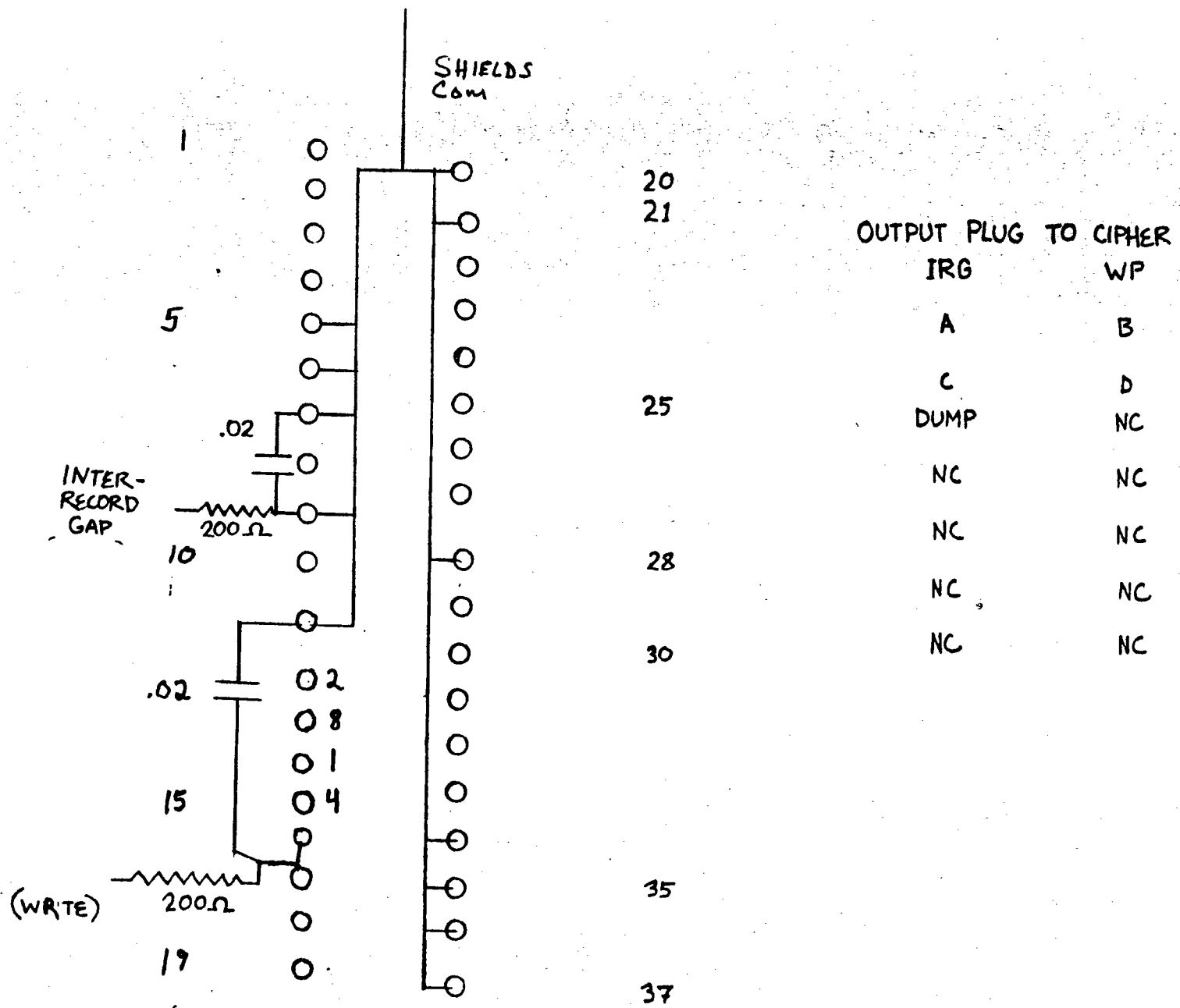


Figure 27: Wiring for Output Plug to the Cipher.

TABLE 8: Characters CDC1700 computer listed for various inputs recorder

Cipher Tapes Input			
T Track Tape			
Representation	Octal *	Computer listed Character	
P 32 16 8 4 2 1	8 1		
o o o 0 0 0 0	0 0	Blank Tape	
1 o o 0 0 0 1	0 1	1	
1 o o 0 0 1 0	0 2	2	
o o o 0 0 1 1	0 3	3	
1 o o 0 1 0 0	0 4	4	
o o o 0 1 0 1	0 5	5	
o o o 0 1 1 0	0 6	6	
1 o o 0 1 1 1	0 7	7	
1 0 0 1 0 0 0	1 0	8	
o o o 1 0 0 1	1 1	9	
o o o 1 0 1 0	1 2	0	zero
1 o o 1 0 1 1	1 3	=	equal
o o o 1 1 0 0	1 4	'	single quote
1 o o 1 1 0 1	1 5	:	colon
1 o o 1 1 1 0	1 6	>	greater than
o o o 1 1 1 1	1 7	"	double quote

TABLE 9: Cipher tape recorder specifications

Power: 120 VAC, 70 watts

Temp: 0° - 40° C

Track: a 7 track tape is generated

Parity: Vertical - odd or even (internally generated)

Horizontal - even (internally generated)

Tape: 1/2" wide, 1.5 mil thick, digital magnetic tape

(IBM standard 7 inch reels) IBM compatible format

Data density: 556 bits per inch

Logical 1: 3.5 - 5.0v

Duration: 10  $\mu$ sec minimum

Tape length: 650 ft.

Max recording time (9 interfaces): ~ 4 days with a 10 minute dump interval



### E. Data Retrieval

Data from the system is currently stored in the Mass Storage System (MSS) of the Lawrence Berkeley Laboratory (LBL) Computer in Berkeley, California. MSS provides very reliable storage while the LBL Computer has an extensively developed software system. Data analysis is done either interactively or on a batch basis using the GEOLAB DATA SYSTEM (See GEOLAB Manual for details) a command oriented software system. Various types of graphical plots and sophisticated data manipulations are possible with minimal effort on the user's part.

#### IV. REFERENCES

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## V. Appendix

## A. Parts Lists

## CMOS CLOCK - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RB-1155	1	Sprague	1.1 m, $\frac{1}{2}$ W, 5%
Potentiometer	3006W-1-204	1	Bourns	200 K
IC	CD4009AE	1	RCA	
IC	CD4020AE	1	RCA	
Capacitor	8121-050-651-473M	1	Erie	.047 $\mu$ , +20%, 50V
Standoffs	2003-B-1	12	USECO	
IC Socket	316-AG39D	2	Augat	16 pin dip socket
PC Board		1		

## MULTIPLEX AND CONTROL - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RA-1035	6	Sprague	10 K, 1/4 w, 5%
Resistor	RA-1045	4	Sprague	100 K, 1/4 w, 5%
Resistor	RA-4725	3	Sprague	4.7 K, 1/4 w, 5%
Resistor	RA-5145	1	Sprague	510 K, 1/4 w, 5%
Resistor	RA-2245	2	Sprague	220 K, 1/4 w, 5%
Resistor	RA-3345	1	Sprague	330 K, 1/4 w, 5%
Resistor	RA-1015	1	Sprague	100 $\Omega$ , 1/4 w, 5%
Capacitor	150D106X9020B2	3	Sprague	10 $\mu$ , 20 VDC, $\pm$ 10%, Solid Tantalum
Capacitor	5855-000-Y5U0-503Z	6	Erie	.05 $\mu$ , 50 V, $\pm$ 20% Disc type
Capacitor	805-000-Z5V0-103Z	3	Erie	.01 $\mu$ , 50 V, $\pm$ 20% Disc type
Transistor	F2N4403	1	Fairchild	
Transistor	2N5976	1	Motorola	
Diode	DT230F	3	General Electric	
IC	CD4009AE	1	RCA	
IC	CD4025AE	1	RCA	
IC	CD4027AE	3	RCA	
IC	SN74LS197N	1	Texas Inst.	
IC	DM74154N	1	National	
Relay	W117DIP-5	16	Magnecraft	200 $\Omega$
PC Board		1		
Socket	314-AG39D	1	Augat	14 pin dip socket
Socket	316-AG39D	2	Augat	16 pin dip socket

## MULTIPLEX AND CONTROL - TRANSMITTER (Cont.)

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Connector Pin	2970-02	17	Cambion	
Header	614-DG6	1	Augat	14 pin plug

## CRYSTAL VCO - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
8 pin DIP Socket	508-AG10D	2	Augat	
16 pin DIP Socket	316 AG39D	3	Augat	
14 pin DIP Socket	314-AG5D-2R	2	Augat	
Transformer	SSO-14	1	UTC/TRW	T-1
Inductor	ML-7 TF5R2022* 6.0 HY	1	UTC	ML-7
Micro Power OP AMP	LM308N	2	National	
Capacitor	.01MFD 100VOC * WMF1S1 CDE+ 10%	1	Cornell-Dubilier	C-2
Capacitor	.027 MFO 100VOC* WMF 1S27 + 10%	1	Cornell-Dubilier	C-1
Resistor	RA 1035	2	Sprague	R-1, R-5, 10K 1/4 watt 5%
Resistor	RA 3015	1	Sprague	R-3, 300 $\Omega$ 1/4 watt, 5%
Resistor	RA 5125	1	Sprague	R-4, 5.1K 1/4 watt, 5%
IC	CD4000AE	1	RCA	
IC	CD4009AE	1	RCA	
IC	CD4018 AE	1	RCA	
IC	CD4012AE	1	RCA	
IC	CD4060AE	1	RCA	
Resistance Pot	50K 43W503	1	Spectrol or Equiv.	R-2
Quartz Crystal	CS-700 15PF	1	Intern'l, Oklahoma City	Specify Freq. in MHz - see catalog
Capacitor	47 PF 10TSQ47	1	Sprague	G-4

\* values for 480 Hz center frequency

## CRYSTAL VCO - TRANSMITTER (Cont.)

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	.22 MF 50V	1	Erie	C-3
Transformer Bracket	SSO-CH	1	UTC/TRW	
PC Board		1		

## DC/DC POWER CONVERTER - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Power Converter	MP 3020	1	ANALOGIC	DC Power Converter
DIODE	IN 753	1	General Electric	Any General purpose silicon diode
Relay	W117 DIP-13	1	Magnecraft	5VDC, 500 $\Omega$
P.C. Board		1		
Socket	314-AG39D	1	Augat	14 pin DIP socket



## LARSE TRANSMITTER BOARD - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Larse-SEN	LCS-171-60-0	1	Larse Corp.	Options: J, K, L, U(DS X, W-10770
A/D Converter Analogic	MP 2412	1	Analogic	
Resistors	RA-1045	2	Sprague	100K, $\frac{1}{2}$ W, 5%
Resistors	RA-1035	5	Sprague	10K, $\frac{1}{2}$ W, 5%
Capacitors	150D106x9020B2	2	Sprague	<u>+</u> 10% Solid 10MF, 20VDC Tantalum
Capacitors	CK06BX104K	1	Erie	100K p <sup>f</sup> , 100V
Capacitors	CK05BX683K	1	Erie	68KPF, 50V <u>+</u> 10%
Transistor	2N3569	1	Fairchild	
IC	LM 310N	1	National	
P.C. Board		1		

## TRANSMITTER BOX

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Transmitter Box	99380	1	Skydyne	
Aluminum Spacers	8344	5	HH Smith	6-32 Hread, .625" length
Connector		2	T + S	Includes rubber insert
Wire	18 guage, Stranded	4	Belden	1 ea; orange, red, yellow, black ~ 18" in length
Spade Lugs	T-2118	6	Waldon	Insulated
Wire	18 guage, stranded	2	Belden	1 ea; red, black ~ 9" in length
MS Connectors	MS-3106-14S-9P	1	Amphenol	
	MS-3106-14S-5S	1	Amphenol	
	MS-3106-14S-5P	1	Amphenol	
	MS-3420-6	2	Amphenol	
	AN-3057-6	2	Amphenol	
Strain Relief Connector	#2520	2	T & B	Specify to include rubber inserts

## MOTHER BOARD - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Connector	2VK22S/2-2	3	Viking	P.C. Socket, 22 conta
Connector	2VK15S/2-2	4	Viking	P.C. Socket, 15 conta
Terminal block	20-140Y	1	Cinch	20 contact terminal strip
Terminal block	5-140Y	1	Cinch	5 contact terminal strip
Terminal block	2-140Y	1	Cinch	2 contact terminal strip
P.C. Board		1		

TOTAL PARTS LIST - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RB1155	1	Sprague	1.1 M $\Omega$ , 1/2 W, 5%
"	RA1035	13	"	10K $\Omega$ , 1/4W, 5%
"	RA1045	6	"	100K $\Omega$ , 1/4W, 5%
"	RA4725	3	"	4.7K $\Omega$ , 1/4W, 5%
"	RA5145	1	"	510K $\Omega$ , 1/4W, 5%
"	RA2245	2	"	220K $\Omega$ , 1/4W, 5%
"	RA3345	1	"	330K $\Omega$ , 1/4W, 5%
"	RA1015	1	"	100 $\Omega$ , 1/4W, 5%
"	RA3015	1	"	300 $\Omega$ , 1/4W, 5%
"	RA5125	1	"	5.1K $\Omega$ , 1/4W, 5%
Potentiometer	3006-1-204	1	Bourns	200K $\Omega$ ,
"	43W503	1	Spectrol or Equiv.	50K $\Omega$
I.C.	CD4009AE	3	RCA	
"	CD4020AE	1	RCA	
"	CD4025AE	1	RCA	
"	CD4027AE	3	RCA	
"	SN74LS197N	1	Texas Instr.	
"	DM74154N	1	National	
"	LM308N	2	National	
"	CD4000AE	1	RCA	
"	CD4018AE	1	RCA	
"	CD4012AE	1	RCA	
"	CD4060AE	1	RCA	
"	LM310	1	National	

TOTAL PARTS LIST - TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	8121-050-651-473M	1	Erie	.047 $\mu$ , 20%, 50V
"	5855-000-Y5U0-503Z	6	Erie	.05 $\mu$ , 20%, 50V disc type
"	150D106X9020B2	5	Sprague	10 $\mu$ , 10%, 20V solid tantalum
"	805-000-Z5V0-103	3	Erie	.01 $\mu$ , 20%, 50V disc type
"	WMF1S1	1	Cornell-Dubilier	C2, .01 $\mu$ , 100V*
"	WMF1S27	1	Cornell-Dubilier	C1, .027 $\mu$ , 100V*
"	10TSQ47	1	Sprague	47pF
"		1	Erie	.22 $\mu$
"	CK06BX104K	1	Erie	.1 $\mu$ , 100V
"	CK05BX683K	1	Erie	.068 $\mu$ , 10%, 50V
I.C. Socket	316-AG39D	7	Augat	16 pin DIP socket
"	314-AG39D	4	Augat	14 pin DIP socket
"	508-AG10D	2	Augat	8 pin DIP socket
Transistor	F2N4403	1	Fairchild	
"	2N5976	1	Motorola	
"	2N3569	1	Fairchild	
Diode	1N753	1	General Electric	Any general-purpose silicon diode
"	DT230F	3	G.E.	
Relay	W117DIP-5	16	Magnecraft	
"	W117DIP-13	1	Magnecraft	5VDC, 500 $\Omega$
Transformer	SS0-14	1	UTC/TRW	

\*Values for 480Hz center frequency.

TOTAL PARTS LIST -- TRANSMITTER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Transformer Bracket	SSO-CH	1	UTC/TRW	
Inductor	ML-7 TF5R2022	1	UTC/TRW	6.0 Henry* ML-7
Quartz Crystal	CS-700 15PF	1	International, Oklahoma City	Specify freq in MHz. See catalogue
Power Converter	MP3020	1	Analogic	DC power converter
A/D Converter	MP2412	1	Analogic	
Larse-Sen	LCS-171-60-0	1	Larse Corp	Options:J,K,U (DS), X, W-10770
Connector Pin	2970-02	17	Cambion	
Header	614-DG6	1	Augat	14 pin plug
Transmitter Box	99380	1	Skydyne	
Aluminum Spacers	8344	5	H.H. Smith	6-32 thread, .625" l.
Wire		4	Beldon	18 gauge stranded 1 each: orange, red yellow, black. 18" l.
Wire		2	Beldon	18 gauge stranded 1 each: red, black 9" l.
Spade Lugs	T2118	6	Waldon	Insulated
MS Connector	MS-3106-14S-9P	1	Amphenol	
"	MS-3106-14S-5P	1	Amphenol	
"	MS-3106-14S-5S	1	Amphenol	
"	MS-3420-6	2	Amphenol	
"	AN-3057-6	2	Amphenol	
Strain Relief Valve	2520	2	T&B	Specify to include rubber inserts.

\*Value for 480HZ center frequency.

TORAL PARTS LIST - TRANSMITTER

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Connector	2VK22S/2-2	3	Viking	P.C. Socket, 22 contacts
Connector	2VK15S/2-2	4	Viking	P.C. Socket, 15 contacts
Terminal Block	20-140y	1	Cinch	20 contact terminal strip
Terminal Block	2-140y	1	Cinch	2 contact terminal strip
P.C. Board		6	Ramlor	

## 2. Receiver

## F.S.K. DISCRIMINATOR - RECEIVER

Component Name*	Part Number	No.	Distributor Manufacturer	Comments
C-1 and C-16	8131-050-651-224M	2	Erie	.22, 50 VDC
C-2, C-3, C-4, C-5	WMF 1S1	4	Cornell-Dubilier	.01, 100 VDC
C-6, C-7, C-9	WMF 1P1	3	Cornell-Dubilier	.1, 100 VDC
C-8	WCRO5S68, 5%	1	Cornell-Dubilier	.068, 50 VDC $\pm$ 5%
C-10	WMF 1D 22	1	Cornell-Dubilier	.0022, 100 VDC
C-11	WMF 1S82	1	Cornell-Dubilier	.082, 100 VDC
C-12, C-13, C-14, C-15	TAPF20- -15/25 50	4	ITT Seimiconductors	15MF, 25 V
C-17	CK05BX 102	1	Erie	1000 pf, 200 V
Transistor Q-1	2N3711	1		
741A, 741B	741H	2	National	
LM304 (IC)	LM304H	1	Teledyne	IC Voltage Regulator
LM305 (IC)	LM305H	1	Teledyne	"
2211 (IC)	XR2211	1	EXAR Integrated Sys.	
7404 (IC)	DM7404	1	National	
T-1 (Transformer)	SSO-2	1	UTC	Transformer
LED	5082-4403	1	Hewlett-Packard	
LED Bracket	5082-4707	1	Hewlett Packard	
P. C. Board		1		P.C. Board

\* NOTE: Component name for discriminator is referenced to parts location diagram only, not to circuit diagram.



## F.S.K. DISCRIMINATOR - RECEIVER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
R-1	43W502	1	Sprague	Potentiometer 5k
R-2	RA-9135	1	"	91K,1/4W,5%
R-3	RA-1025	1	"	1K,1/4W,5%
R-4	RA-1035	1	"	10K,1/4W,5%
R-5	RA-5625	1	"	5-6K,1/4W,5%
R-6	RA-5635	1	"	56K,1/4W,5%
R-7	RA-5125	1	"	5.1K,1/4W,5%
R-8	RA-5145	1	"	510K,1/4W,5%
R-9	RA-1045	1	"	100K,1/4W,5%
R-10	RA-3645	1	"	360K,1/4W,5%
R-11	RA-3035	1	"	30K,1/4W,5%
R-12	3059L-1-202 2K	1	Bourns, Inc.	Potentiometer 2K
R-14 and R-29	RA-1005	2	Sprague	1056,1/4W,5%
R-15	RA-3925	1	"	3.9K,1/4W,5%
R-15 and R-18	RA-7525	2	"	7.5K,1/4W,5%
RLED	RA-3915	1	"	39052,1/4W,5%
R-26 and R-27	RNC65H3573FM	2	Corning	3.571K,1/4W,1%
R-1A* and R-1B*	RA-1335	2	Sprague	13K,1/4W,5%
R-2A*	RA-1325; RA-1925	lea.	"	1.3K and 1.9K,1/4W,5%
R-2B*	RA-1325; RA-2725	lea.	"	1.3K and 2.7K,1/4W,5%
R-3A* and R-3B*	RC07CB135J	2	Allen-Bradley	1.3Meg.,1/4W,5%

\* Values of these resistors depends on desired frequency. Above for 480 Hz

## F.S.K. DISCRIMINATOR - RECEIVER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Socket (10 pin)	8058-1G34	1	Augat	10-pin transistor socket
Socket (8 pin)	8058-1G50	3	Augat	8-pin transistor socket
IC Socket	314-AG5D-28	2	Augat	14 pin dip socket
Test Jack	63-1005-102	1	H.H. Smith	Red
Test Jack	63-1005-105	1	H.H. Smith	Blue
Front Panel		1		
Screws		2		4-40 x 1/8" steel w/nuts

## BACK PLANE - RECEIVER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Dip socket	316-AG39D	18	Augat	16 pin dip socket
terminal strip	5-140Y	1	Cinch/TRW	5 connections
" "	4-140Y	1	" "	4 connections
" "	20-140Y	1	" "	20 connections
P.C. Socket	3-583679-8	10	Amp Special Indus- tries	40 contact socket for P.C. Board
P. C. Board		1		

## DUAL LATCH-DAC-RECEIVER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	150D156X9020B2	2	Sprague	15 $\mu$ , 10%, 20 VDC Solid Electro.
"	150D476X9006B2	1	"	47 $\mu$ , 10%, 6 VDC Solid Electro.
IC	DM 74154	4	National	
Digital-Analog Converter	$\mu$ Verter ZD429	2	Zeltex	
Test Jacks	105-0750-001	2	E. F. Johnson	Horizontal type
Card Ejector	SAE 6100	1	Stanford Applied Engineering	
Card Puller	SAE 6200	1	Stanford Applied Engineering	
Screws/nuts		2	H. H. Smith (or equiv)	4-40x $\frac{1}{2}$ " binding machine screws; 4-40 screws
P.C. Board		1		

## LARSE: CONVERT LOGIC - RECEIVER

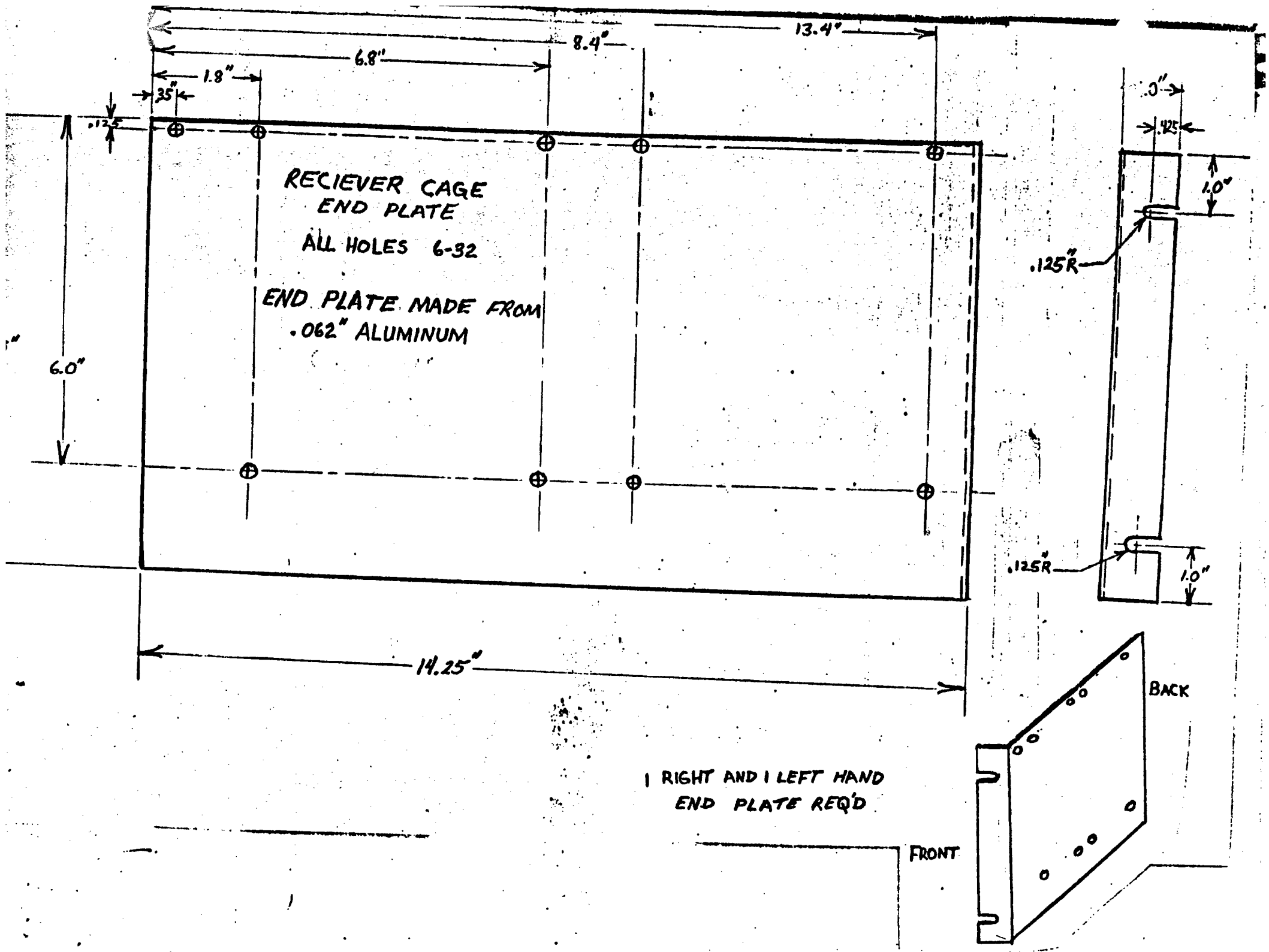
Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RA-1035	18	Sprague	10K, $\frac{1}{4}$ W, 5%
"	RA-3315	2	"	330 $\Omega$ , $\frac{1}{4}$ W, 5%
Capacitor	150D156X9020B2	1	"	15 $\mu$ + 10%, 20 VDC Solid Elect.
"	150D476X9035	1	"	47 $\mu$ + 10%, 35 VDC Solid Elect.
"	5 GA -S10	1	"	.01 $\mu$ , 500 V disc.
"	5GA-D10	1	"	.001 $\mu$ , 1KV disc.
Data Communica- tor	REDE LCR 271-60-0 Options: A, B, E, F, I, M, N, X	1	Larse Corp.	
IC	DM 74154N	1	National	
"	DM8563N/DM74193N	3	"	
"	DM74160N	4	"	
"	DM74121N	1	"	
"	DM7400	2	"	
Test Jacks	105-0750-001	3	E. F. Johnson	Horizontal type
Card Ejector	SAE 6100	1	Stanford Applied Eng.	
Card Puller	SAE 6200	1	Stanford Applied Eng.	
Screws/nuts		2	H.H. Smith (or equiv.)	4-40x $\frac{1}{4}$ " binding machine screws; 4-40 nuts
P.C. Board		1		

## SUMMER BOARD - RECEIVER

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor				
"	RA-2735	3	Sprague	27K, ½W, 5%
"	RA-1035	6	"	10K, ½W, 5%
"	RA-4715	2	"	470Ω, ½W, 5%
Capacitor	150D156X9020B2	3	Sprague	15μ, 20 BDC, Solid Electro.
"	WMF 1D15, 100 VDC	1	Cornell-Dubilier	.0015μ ± 10%, 100V
"	WMF 1S22, 100 VDC	1	" "	.022μ ± 10%, 100V
"	WMF 1S1, 100 VDC	1	" "	.01μ ± 10%, 100V
Diode	1N914	2	Motorola	250m A.
IC	LM741CN	2	National	
IC Socket	308-AG39D	2	Augat	8 pin DIP socket, low profile
Connector	3AH15/1JN5	1	Viking	30 pin female connect.
P.C. Board		1	Ramlar	
Card Ejector	SAE 6100	1	Stanford Applied Engr.	For P.C. Board
Card Puller	SAE 6200	1	Stanford Applied Eng.	For P.C. Board
Screws/nuts		4		4-40x¼", binding head; 4-40 nuts

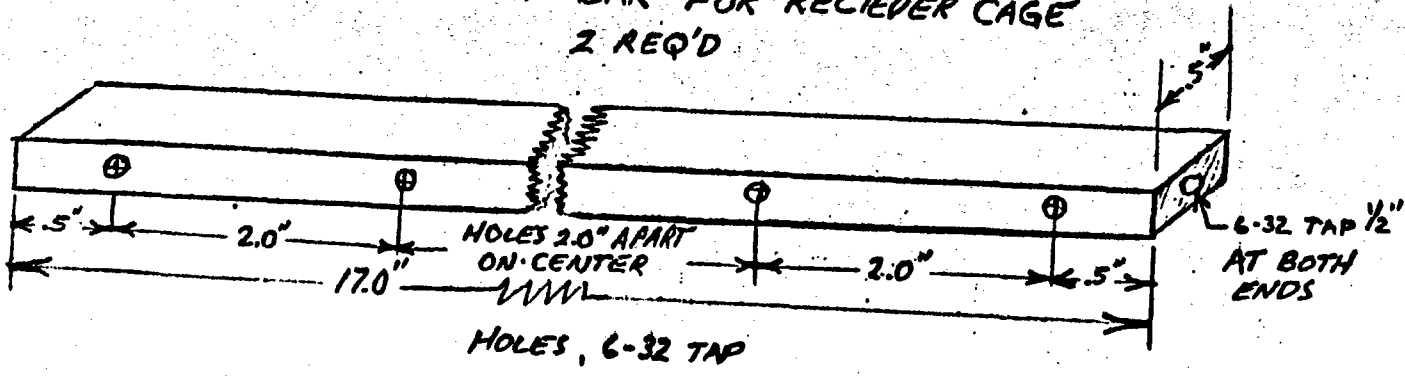
## RECEIVER CAGE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Locking tab card guide	SAE 1650	40	Stanford Applied Engr.	
I.D. Locking tabs	SAE 3100	10	" " "	
Locking tabs	SAE 3000	70	" " "	
Support bar	SAE 4050	8	" " "	
Screws		38		6-32 x 1/4" binding head machine screws
Support bar	Not a stock item, see diagram	2		
End Plates	Not a stock item, see diagram	2		1 left hand, 1 right har
*Note Receiver Cage contains:			1 FSK Discriminator w/o threshold card	
			1 Larse: Convert Logic card	
			8 Dual Latch, DAC cards	
			1 Back Plane P.C. Board	





SUPPORT BAR FOR RECIEVER CAGE  
2 REQ'D



TOTAL PARTS LIST - RECEIVER

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Resistor	RA9135	1	Sprague	91k $\Omega$ , 1/4W, 5%
"	RA1025	1	"	1K $\Omega$ , 1/4W, 5%
"	RA1035	25	"	10K $\Omega$ , 1/4W, 5%
"	RA5625	1	"	5.6K $\Omega$ , 1/4W, 5%
"	RA5635	1	"	56K $\Omega$ , 1/4W, 5%
"	RA5125	1	"	5.1K $\Omega$ , 1/4W, 5%
"	RA5145	1	"	510K $\Omega$ , 1/4W, 5%
"	RA1045	1	"	100K $\Omega$ , 1/4W, 5%
"	RA3645	1	"	360K $\Omega$ , 1/4W, 5%
"	RA3035	1	"	30K $\Omega$ , 1/4W, 5%
"	RA1005	2	"	10 $\Omega$ , 1/4W, 5%
"	RA3925	1	"	3.9K $\Omega$ , 1/4W, 5%
"	RA7525	2	"	7.5K $\Omega$ , 1/4W, 5%
"	RA3915	2	"	390 $\Omega$ , 1/4W, 5%
"	RNC65H3573FM	2	Corning	3.571K $\Omega$ , 1/4W, 5%
"	RA1335	2	Sprague	13K $\Omega$ , 1/4W, 5%*
"	RA2725	1	"	2.7K $\Omega$ , 1/4W, 5%*
"	RA1325	1	"	1.3K $\Omega$ , 1/4W, 5%*
"	RC07CB135J	2	Allen-Bradley	1.3M $\Omega$ , 1/4W, 5%*
"	RA3315	2	Sprague	330 $\Omega$ , 1/4W, 5%
"	RA2735	3	"	27K $\Omega$ , 1/4W, 5%
"	RA4715	2	"	470 $\Omega$ , 1/4W, 5%
Potentiometer	43W502	1	"	5K $\Omega$ , 1/4W, 5%
"	3059L-1-202	1	Bourns,	2K $\Omega$ , 1/4W, 5%

\* Values depend on desired frequency.

TOTAL PARTS LIST - RECEIVER

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Capacitor	150D476X9035	1	Sprague	47 $\mu$ F, 10%, 35V
"	5GA-S10	1	"	.01 $\mu$ F, 500V disc.
"	5GA-D10	1	"	.001 $\mu$ F, 1KV disc
"	WMF 1D15	1	Cornell-Dubilier	.0015 $\mu$ F, 10%, 100V
"	WMF 1S22	1	" "	.022 $\mu$ F, 10%, 100V
I.C. Socket	8058-1G34	1	Augat	10-pin transistor socket
"	8058-1G50	3	"	8-pin transistor socket
"	314-AG5D-28	2	"	14-pin DIP socket
"	316-AG39D	18	"	16-pin DIP socket
"	308-AG39D	2	"	8-pin DIP socket
Transistor	2N3711	1		
Diode	1N914	2	Motorola	250mA
LED	5082-4403	1	Hewlett-Packard	
LED Bracket	5082-4707	1	" "	
Transformer	SS0-2	1	UTC	
Digital-Analog Converter		2	Zeltex	
Data Communicator		1	Larse Corp.	REDE LCR 271-60-0. Options: A, B, E, F, I, M, N, X.
Test Jack	63-1005-102	1	H.H. Smith	Red
" "	63-1005-105	1	H.H. Smith	Blue
" "	105-0750-001	3	E.F. Johnson	Horizontal type

TOTAL PARTS LIST - RECEIVER

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
I.C.	LM304H	1	Teledyne	Voltage Regulator
"	LM305H	1	"	" "
"	XR2211	1	EXAR Integrated Systems	FSK Demodulator
"	DM7404	1	National	
"	LM741H	2	National	
"	DM74154	5	"	
"	DM8563N/DM74193N	3	"	
"	DM74160	4	"	
"	DM74121N	1	"	
"	DM7400	2	"	
"	LM741 CN2	2	"	
Capacitor	8131-050-651-224M	2	Erie	.22 $\mu$ F, 50V
"	WMF 1S1	5	Cornell-Dubilier	.01 $\mu$ F, 100V
"	WMF 1P1	3	" "	.1 $\mu$ F, 100V
"	WCR05S68	1	" "	.068 $\mu$ F, 50V, 5%
"	WMF 1D22	1	" "	.0022 $\mu$ F, 100V
"	WMF 1S82	1	" "	.082 $\mu$ F, 100V
"	TAPF20-15/25 50	4	ITT Semiconductor	15 $\mu$ F, 25V
"	CK05BX 102	1	Erie	1000pF, 200V
"	150D156X9020B2	6	Sprague	15 $\mu$ F, 20V, 10% solid electrolytic
"	150D476X9006B2	1	"	47 $\mu$ F, 6V solid electrolytic

TOTAL PARTS LIST - RECEIVER

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Terminal Strip	5-140y	1	Cinch/TRW	5 connections
" "	4-140y	1	"	4 connections
" "	20-140y	1	"	20 connections
P.C. Socket	3-583679-8	10	Amp Special Industries	40 contact socket for P.C. board
Front Panel		1		
Card Ejector	SAE 6100	3	Stanford Applied Engineering	
Card Puller	SAE 6200	3	Stanford Applied Engineering	
Connector	3AH15/1JN5	1	Viking	30-pin female
Screws		2		4-40x1/8 steel w/ nuts
"		6	H.H. Smith	4-40x1/4 binding machine screws
"		38	H.H. Smith	6-32 binding head machine screw
P.C. Board		4		
Locking tab Card Guide	SAE 1650	40	Stanford Applied Engineering	
I.D. Locking Tabs	SAE 3100	10		
Locking Tabs	SAE 3000	70		
Support Bar	SAE 4050	8		
Support Bar	Not a stock item, see diagram	2		
End Plates	Not a stock item, see diagram	2		one left-hand one right-hand

## 3. Interface

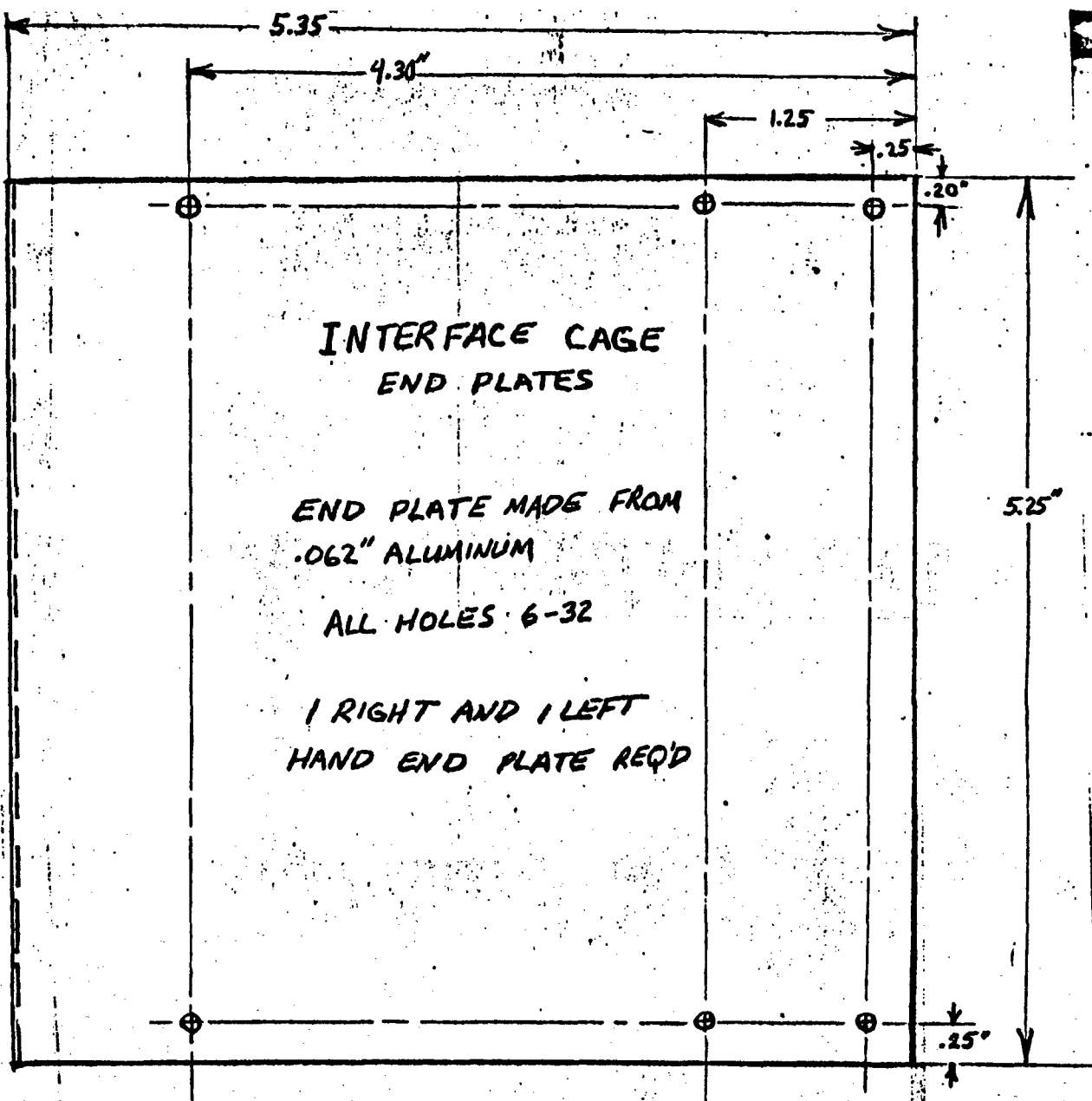
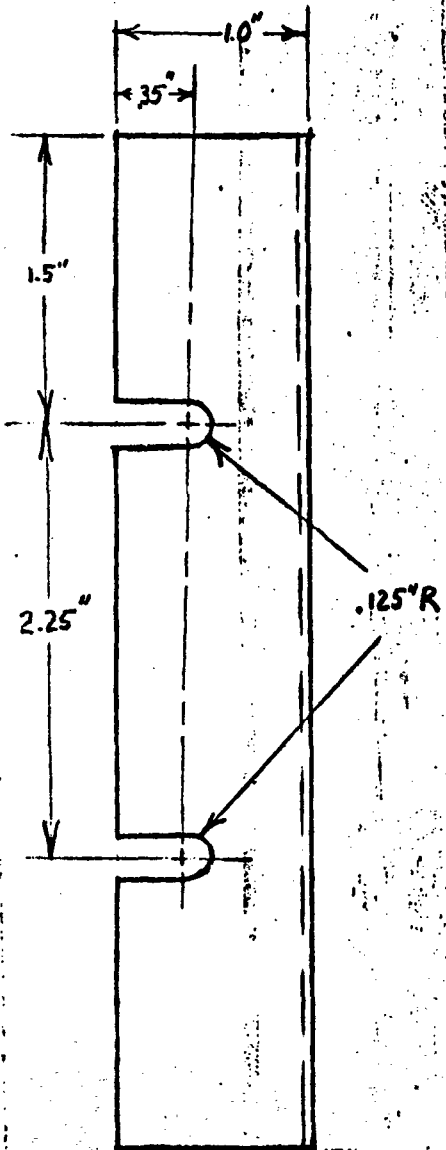
78

## BACK PLANE - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Connectors	2VH22/1AV5	18	Viking	22 contact socket for P.C. Board
"	10-174	1	Cinch	10-contact terminal strip, single row
I. C. Socket	316-AG39D	15	Augat	Low profile 16-pin socket
Capacitor	WCR 05S68	1	Cornell & Dubilier	.068 $\mu$ , $\pm$ 5%, 50VDC
P.C. Board		1	Ramlar	

## CAGE 1 - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Locking Tab Card Guide	SAE 1450	36	Stanford Applied Eng	
I.D. Locking Tabs	SAE 3100	18	" " "	
Locking Tabs	SAE 3000	108	" " "	
Support bar	SAE 4050	6	" " "	
Connector foot	SAE 2359	18	" " "	
End Plates	Not a stock item (see attached drawing)	2		See diagram for details





## DATA BOARD - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RA-2225	3	Sprague (or equiv.)	2.2K, $\frac{1}{4}$ W, 5%
Capacitor	150D606X9006B2	1	Sprague (or equiv.)	60 $\mu$ , + 10%, 6VDC, Solid Tantalum
Transistor	F2N3904	1	"	
IC	SN7401N	7	Texas Instrument	
IC	DM 7442N	1	National	
IC	7404	1		
P.C. Board		1	Ramlar	
Card Puller	SAE 6200	1	Stanford Applied Eng.	
Card Ejector	SAE 6100	1	" " "	
Screws/nuts		2		6-32 x $\frac{1}{4}$ " binding head

## DAY-TIME CODE - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistors	RA-1035	4	Sprague	10 K, $\frac{1}{2}$ W, 5%
"	RA-1515	1	Sprague	150 $\Omega$ , $\frac{1}{2}$ W, 5%
LED	5082-4850	4	Hewlett-Packard	
IC	DM 7401	5	National	
IC	DM 7417	1	National	
IC	DM 7420	1	National	
IC	DM 7400	1	National	
Card Ejector	SAE 6100	1	Stanford Applied Eng.	
Card Puller	SAE 6200	1	" " "	
Capacitor	150D686X9006R2	1	Sprague	6 VDC, 68 $\mu$ , $\pm$ 10% Solid Tantalum
IC	DM 7420	1	National	
Screws/nuts		2		6-32 x $\frac{1}{4}$ " binding head
P.C. Board				

## SEQUENCER - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RA-1035	2	Sprague (or equiv.)	10 K, $\frac{1}{4}$ W, 5%
"	RA-2735	2	Sprague (or equiv.)	27 K, $\frac{1}{4}$ W, 5%
"	RA-4325	1	Sprague (or equiv.)	4.3 K, $\frac{1}{4}$ W, 5%
"	RA-4745	1	Sprague	470 K, $\frac{1}{4}$ W, 5%
Capacitor	8121-100 W5R0 103 K	6	Erie (or equiv.)	.01 $\mu$ , 100V, $\pm$ 10%, Disc.
Capacitor	150D686X9006R2	1	Sprague	68 $\mu$ , 6VDC $\pm$ 10%, Solid Tantalum
IC	DM74154N	2	National (or equiv.)	
"	DM 7404	2	National	
"	DM7493	2	"	
"	DM7420	1	"	
"	DM7400	1	"	
"	DM74107 N	1	"	
"	DM74123	2	"	
"	DM74 121 N	1	"	
P.C. Board		1	Ramlar	
Card Puller	SAE 6200	1	Stanford Applied Eng.	
Card Ejector	SAE 6100	1	" " "	
Screws/nuts		2		6-32 x $\frac{1}{4}$ " binding head

## TIME OF DAY - INTERFACE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	150D686X9006R2	1	Sprague	68 $\mu$ , 6 VDC $\pm$ 10%, Solid Tantalum
IC	SN 7401 N	5	Texas Instrument	
IC	DM7400	1	National	
P. C. Board		1	Ramlar	
Card Puller	SAE 6200	1	Stanford Applied Eng.	
Card Ejector	SAE 6100	1	" " "	
Screws/nuts		2		6-32 x $\frac{1}{4}$ " binding head

TOTAL PARTS LIST - INTERFACE

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Resistor	RA2225	3	Sprague	2.2K $\Omega$ , 1/4W, 5%
"	RA1035	6	"	10K $\Omega$ , 1/4W, 5%
"	RA1515	1	"	150 $\Omega$ , 1/4W, 5%
"	RA2735	2	"	27K $\Omega$ , 1/4W, 5%
"	RA4325	1	"	4.3K $\Omega$ , 1/4W, 5%
"	RA4745	1	"	470K $\Omega$ , 1/4W, 5%
I.C.	SN7401	7	Texas Instruments	
"	DM7442N	1	National	
"	DM7404	3	"	
"	DM7401	6	"	
"	DM7417	1	"	
"	DM7400	3	"	
"	DM7420	2	"	
"	DM74154	2	"	
"	DM7493	2	"	
"	DM74107N	1	"	
"	DM74123	2	"	
"	DM74121	1	"	
Capacitor	WCR 05S68	1	Cornell-Dubilier	.068 $\mu$ , 5%, 50V
"	150D606X9006B2	1	Sprague	60 $\mu$ , 10%, 6V Solid tantalum
"	150D686X9006R2	3	Sprague	68 $\mu$ , 10%, 6V Solid tantalum
"	8121-100 W5R0	6	Erie or equiv.	.01 $\mu$ , 10%, 100V
Transistor	F2N3904	1	Fairchild	

TOTAL PARTS LIST - INTERFACE

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
LED	5082-4850	4	Hewlett-Packard	
Connector	2VH22/1AV5	18	Viking	22 contact for p.c. board
"	10-174	1	Cinch	10 contact terminal, single row
I.C. Socket	316-AG39D	15	Augat	Low profile 16 pin socket
Card Puller	SAE 6200	4	Stanford Applied Engineering	
Card Ejector	SAE 6100	4	" "	
Screws/nuts		9		6x32x1/4 binding head
Locking Tab Card Guide	SAE 1450	36	Stanford Applied Engineering	
I.D. Locking Tabs	SAE 3100	18	" "	
Locking Tabs	SAE 3000	108	" "	
Support Bar	SAE 4050	6	" "	
Connector Foot	SAE 2359	18	" "	
End Plates	not a stock item	2		See diagram for details
P.C. Board		4		

## BACK PLANE - CASCADE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistors	RA-5625	6	Sprague	5.6 K, $\frac{1}{4}$ W, 5%
IC	DM 7404	1	National	
Connectors	143-015-03	2	Amphenol	15 contact socket
Terminal block	2-540	1	Cinch	2 contact terminal strip
Socket	316-AG39D	33	Augat	16 pin dip socket
Socket	314-AG39D	1	"	14 pin dip socket
Socket	508-AG11D	7	"	8 pin dip socket
P.C. Board		1	Ramlar	
P.C. Board Socket	2VH22/1AV5	7	Viking	

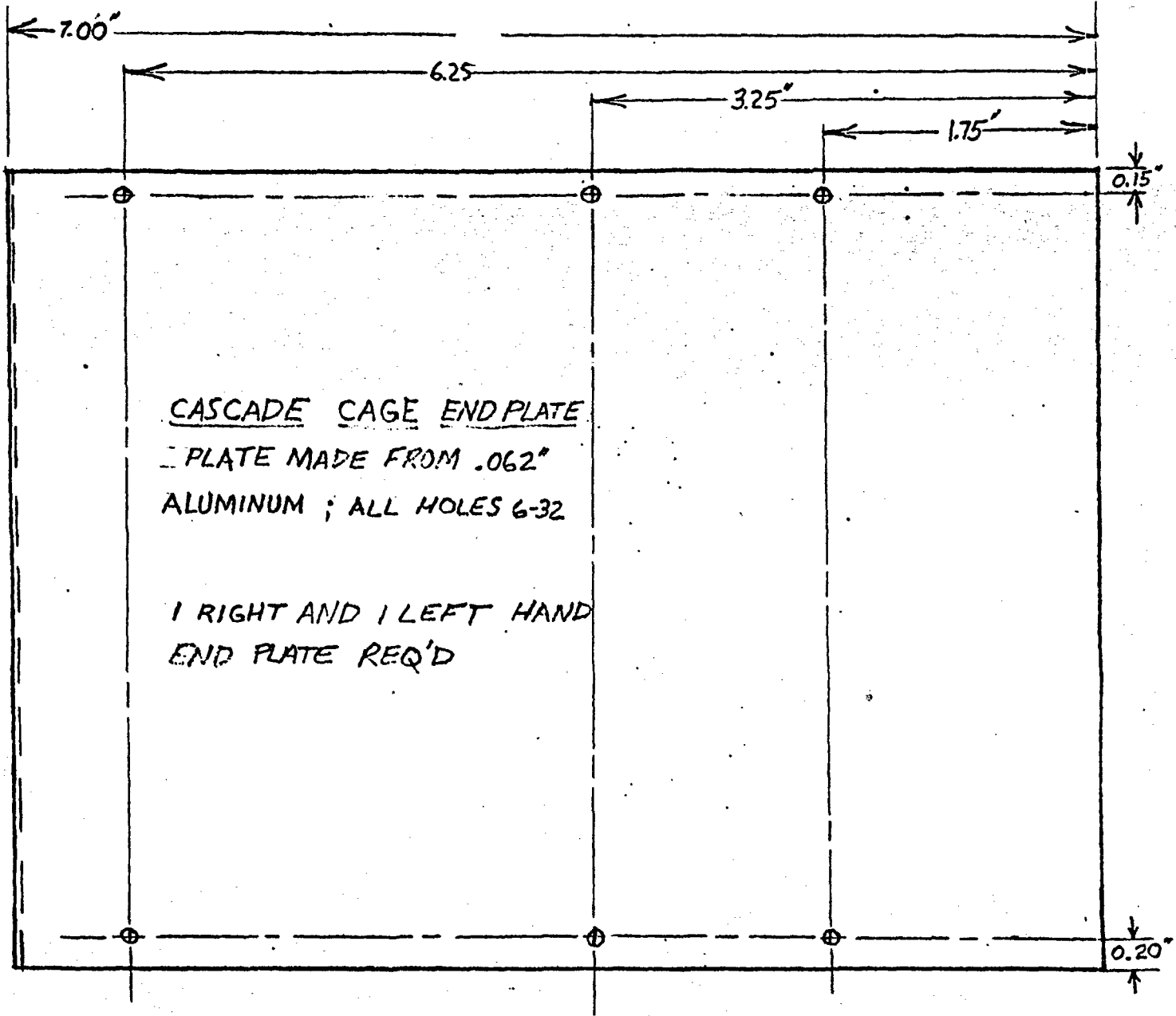
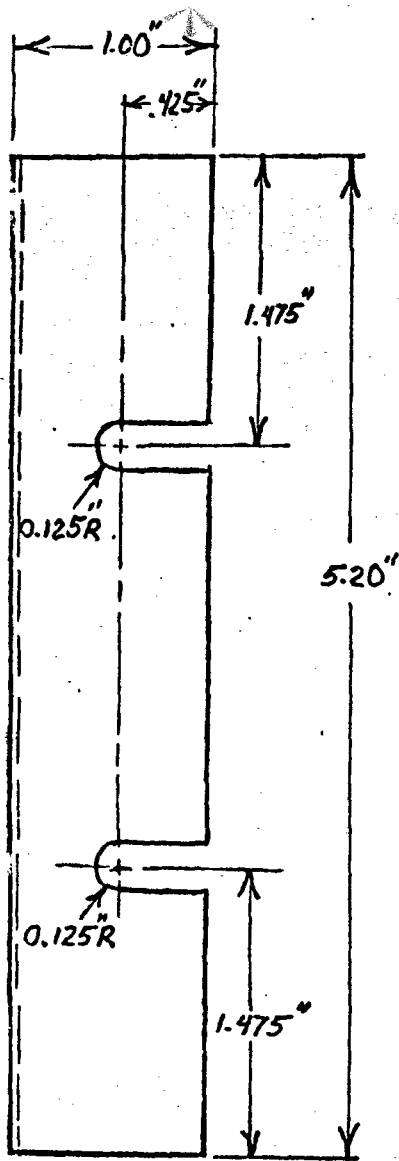
## TIME EXPANDER - CASCADE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	150D606X9006B2	1	Sprague	60 $\mu$ , 6VDC Solid Tantalum
IC	DM7404	6	National	
P.C. Board		1	Ramlar	
Socket	314-AG39D	6	Augat	14 pin dip socket



## · CASCADE CAGE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Locking Tab Card Guide	SAE 1450	14	Stanford Applied Eng.	
I.D. Locking Tabs	SAE 3100	7	" " "	
Locking Tabs	SAE 3000	42	" " "	
Connector Foot	SAE 2359	7	" " "	
End Plates	Not a stock item (See diagram)	2		
Support Bar	SAE 4050	6	Stanford Applied Eng.	



## GATE - CASCADE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor	500D506G025CC7	1	Sprague	50 $\mu$ , 25 VDC Aluminum Electrolytic
IC	DM 7401 N	10	National	
IC	DM 7404	1	"	
P.C. Board		1	Ramlar	
Socket	314-AG39D	11	Augat	14 pin dip socket

## CASCADE CARD - CASCADE

Component Name	Part Number	No.	Distributor Manufacturer	Comments
Resistor	RA-1025	1	Sprague	1 K, 1/4W, 5%
"	RA-3005	1	"	30Ω, 1/4 W, 5%
"	RA-1015	1	"	100Ω, 1/4W, 5%
Capacitor	500D506G025CC7	1	Sprague	50μ, 25 VDC Aluminum Electrolytic
"	CK05BX103K	1	Erie	10,000 pf
LED	5082-4881	10	Hewlett-Packard	
IC	7404	3	National	
"	7400	1	"	
"	DM7420 N	2	"	
"	DM7417 N	2	"	
"	DM7493 N	1	"	
"	DM7442 N	1	"	
Transistor	2N 3569	1	"	
P.C. Board		1	Ramtar	
Socket	316-AG 39D	1	Augat	16 pin dip socket
Socket	314-AG 39D	9	Augat	14 pin dip socket

## CIPHER PLUG - CASCADE-CIPHER

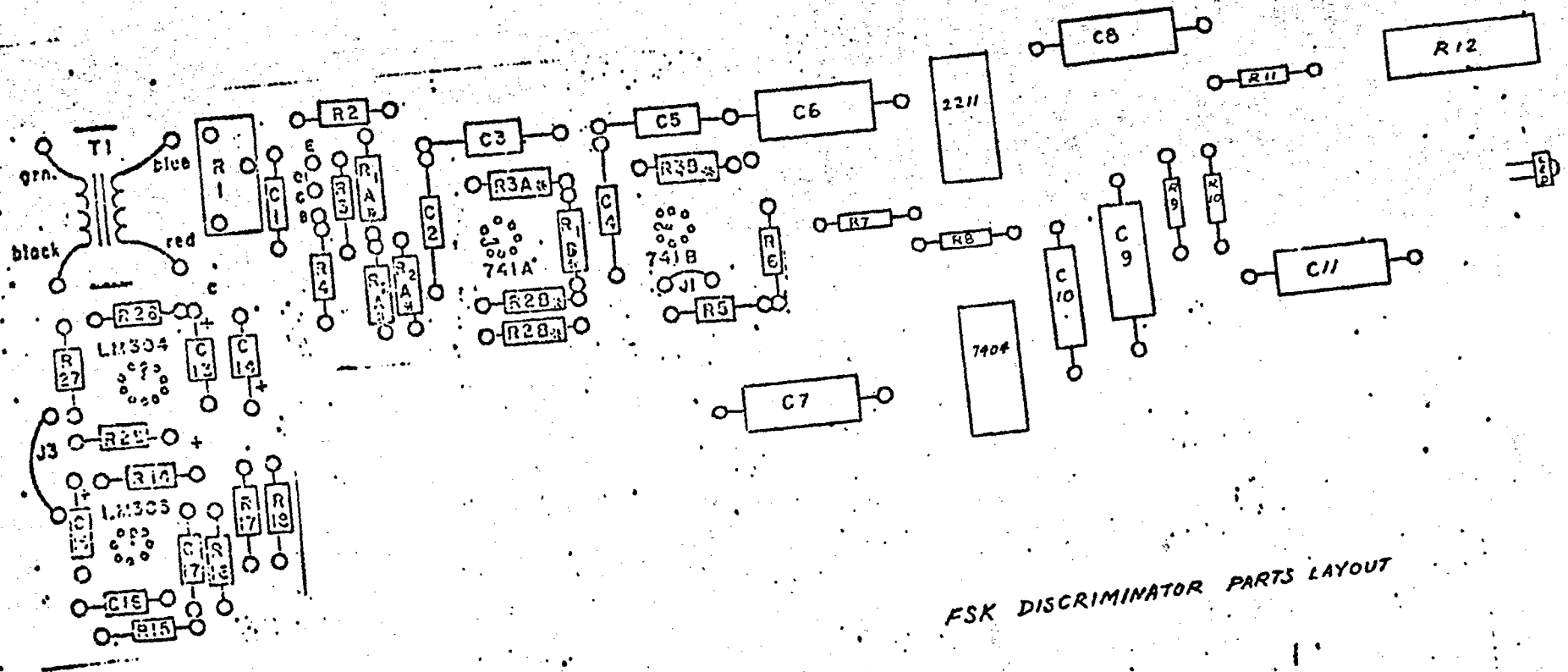
Component Name	Part Number	No.	Distributor Manufacturer	Comments
Capacitor		2	Erie	.22 $\mu$
Resistor	RA-2015	2	Sprague	200 $\Omega$ , $\frac{1}{4}$ W, 5%
Plug		1	Amphenol	

TOTAL PARTS LIST - CASCADE UNIT

Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
Resistor	RA5625	6	Sprague	5.6K $\Omega$ , 1/4W, 5%
"	RA1025	1	"	1K $\Omega$ , 1/4W, 5%
"	RA1015	1	"	100 $\Omega$ , 1/4W, 5%
"	RA2015	2	"	200 $\Omega$ , 1/4W, 5%
I.C.	DM7404	2	National	
"	DM7401	10	"	
"	DM7400	1	"	
"	DM7420	2	"	
"	DM7417	2	"	
"	DM7493	1	"	
"	DM7442N	1	"	
Capacitor	150D606X9006B2	1	Sprague	60 $\mu$ , 6V Solid tantalum
"	500D506G025CC7	2	"	50 $\mu$ , 25V Alum. Electrolytic
"	CK05BX103K	1	Erie	10,000 $\mu$ F
"		2	"	.22 $\mu$ ,
I.C. Socket	316-AG39D	34	Augat	16 pin DIP
"	314-AG39D	27	"	14 pin DIP
"	508-AG11D	7	"	8 pin DIP
Transistor	2N3569	1	National	
LED	5082-4881	10	Hewlett-Packard	
Connector	143-015-03	2	Amphenol	15 contact socket
Terminal Block	2-540	1	Cinch	2 contact strip terminal
Plug		1	Amphenol	1

TOTAL PARTS LIST - CASCADE UNIT

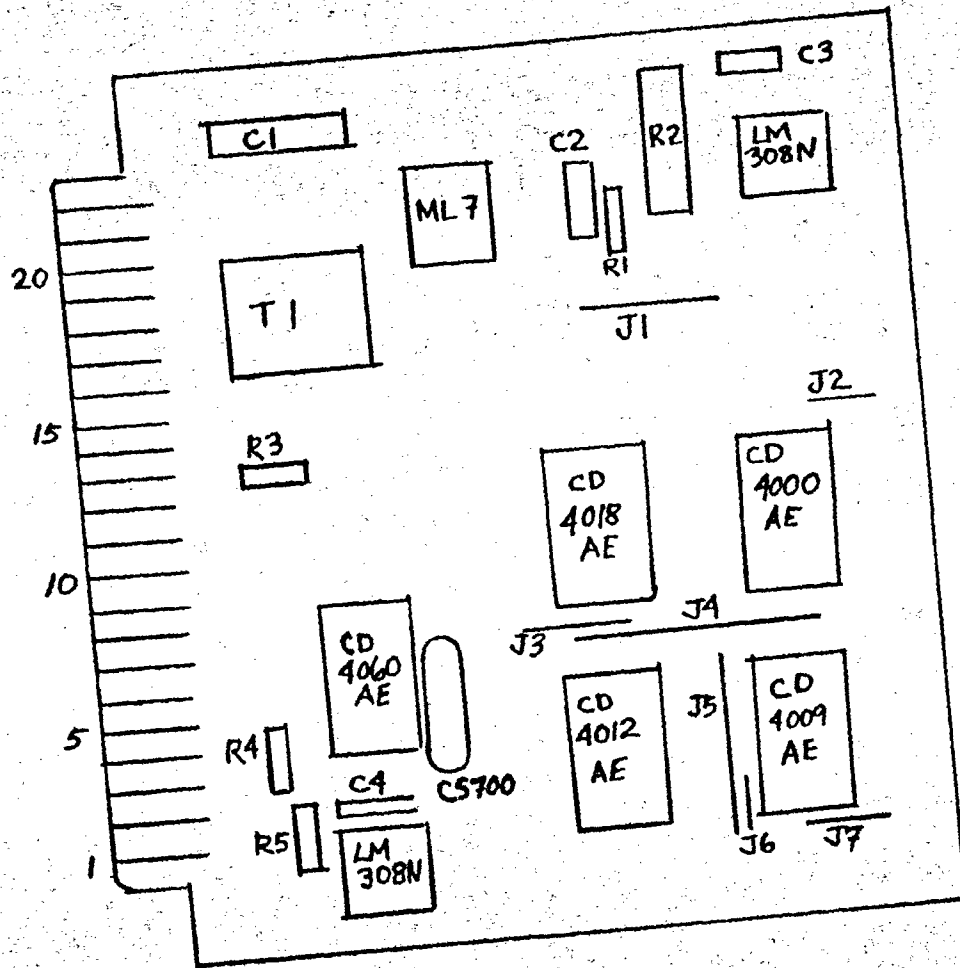
Component Name	Part Number	No.	Distributor/ Manufacturer	Comments
P.C. Board Socket	2VH/1AV5	7	Viking	
Locking Tab Card Guide	SAE 1450	14	Stanford Applied Engineering	
I.D. Locking Tabs	SAE 3100	7	" "	
Locking Tabs	SAE 3000	42	" "	
Connector Foot	SAE 2359	7	" "	
End Plates	not a stock item (see diagram)	2		
Support Bar	SAE 4050	6	" "	
P.C. Board		4		



FSK DISCRIMINATOR PARTS LAYOUT

B. Circuit Components Location Diagrams - 1. Discriminator



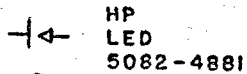
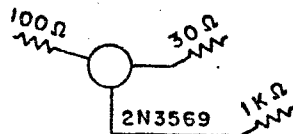
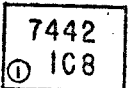
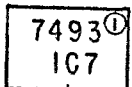
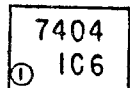
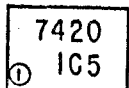
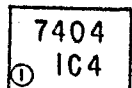
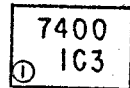
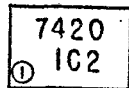
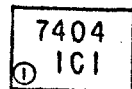


2. VCO Component Location Diagram.

CASCADE

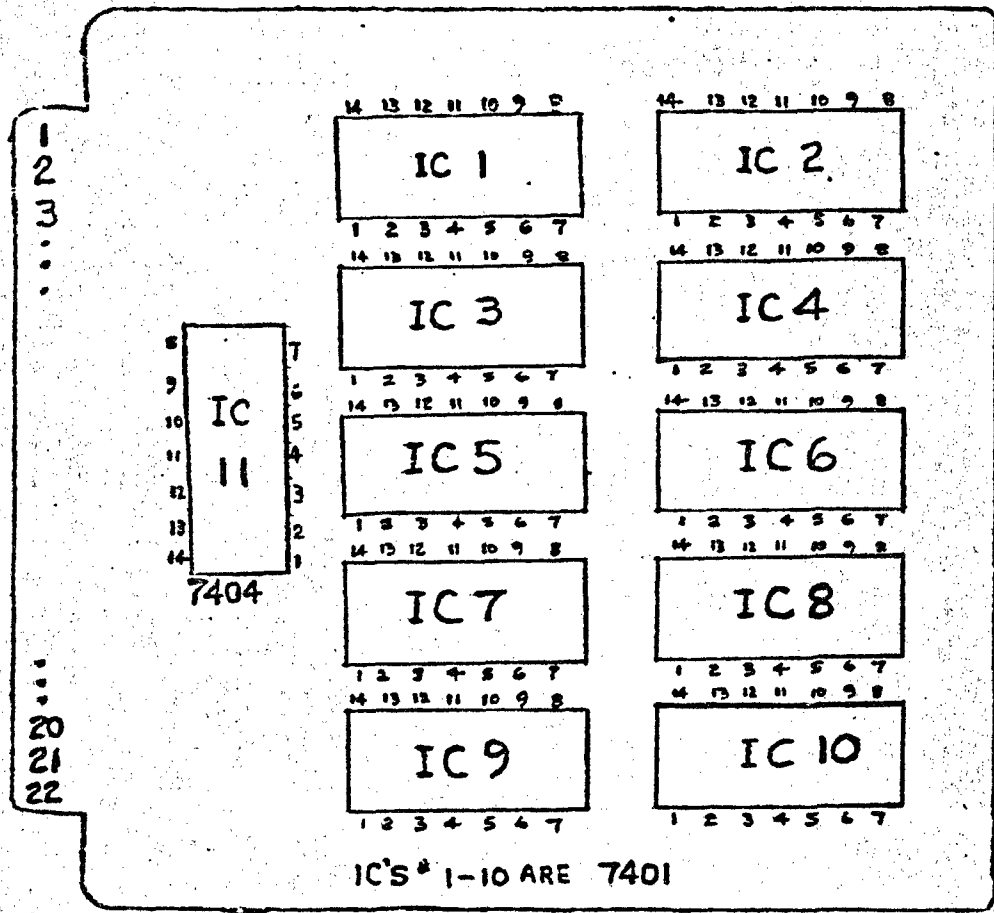
NOTE: THE TRANSISTOR BUFFERS THE TIME LOGIC AND THE COUNTING LOGIC TO REMOVE EXTRANEIOUS PULSES.

RED (COMPONENT)	BLUE (BOTTOM)	BLUE	RED
		A	Z
15B	15A	↓	22
15D	15C	↓	
105B	105A	↓	
105D	105C	↓	
1MA	1MB	↓	
	1MC	↓	



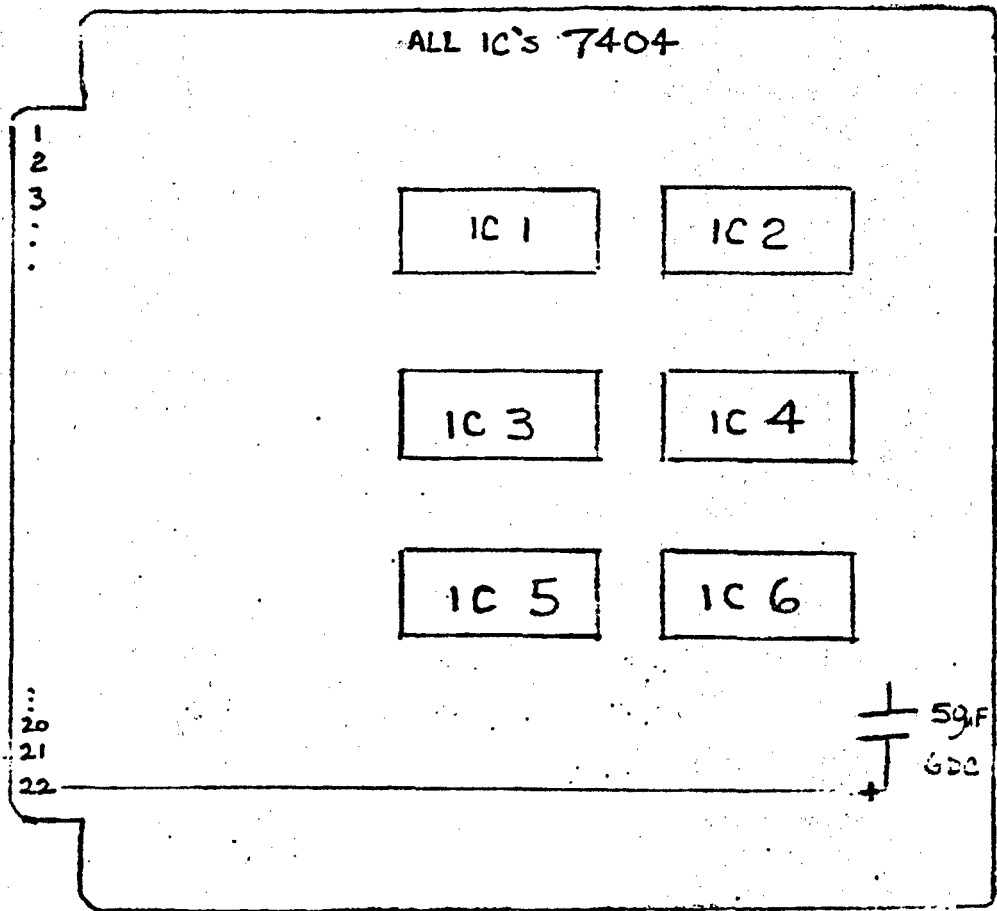
GND  
+5 V

# GATE CARD



# TIME EXPANDER

COMPONENT SIDE = NOS. } EDGE CONNECTOR PINOUTS  
BACKSIDE = LETTERS }



### C. Cascade logic

The Boolean or logic function  $f$ , as seen by the base of the NPN transistor is:

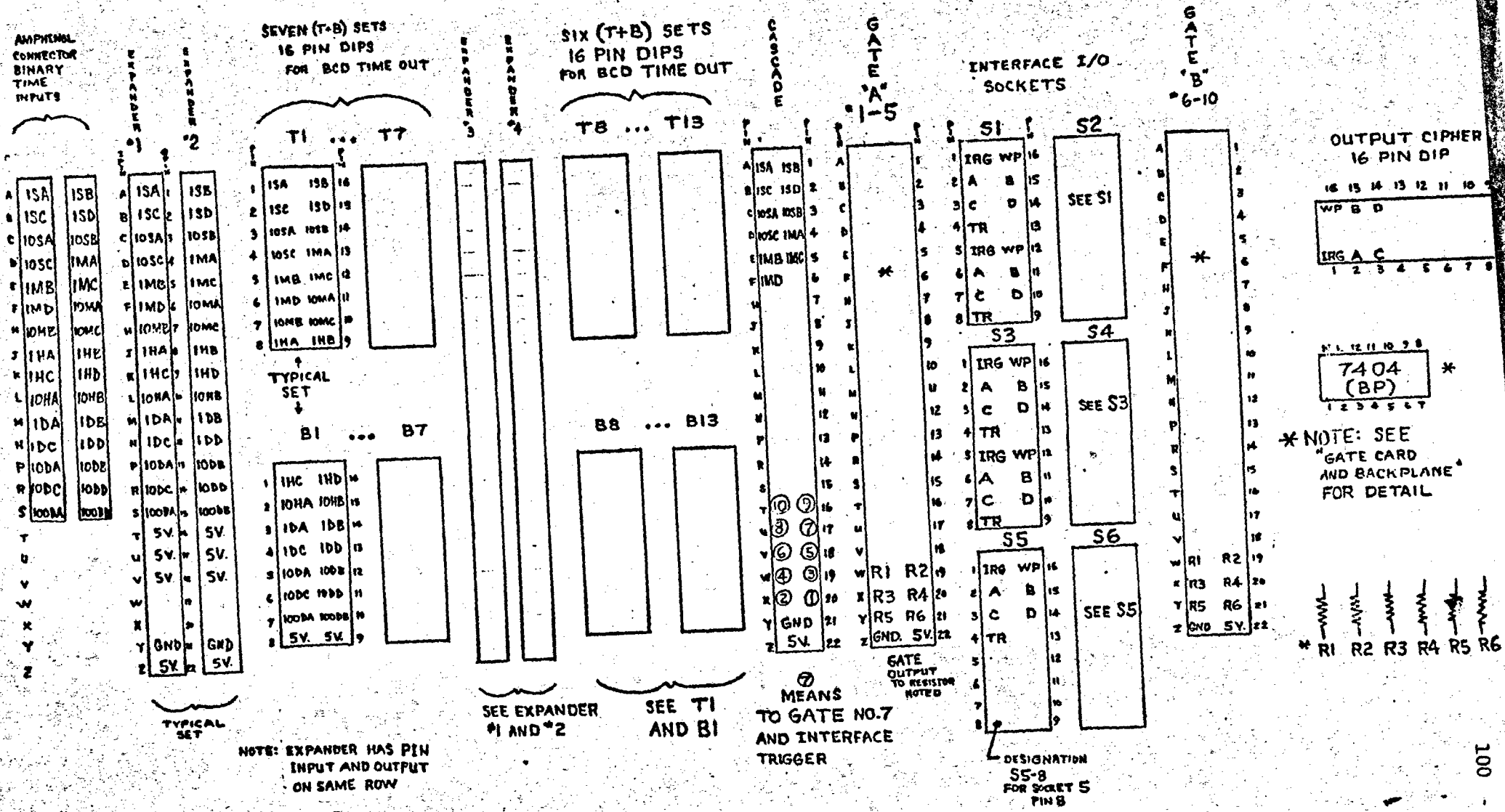
$$f = (A_1 + B_1 + C_1 + D_1) (A_1' + B_1 + C_1' + D_1) + A_3 + B_3 + C_3 + D_3$$

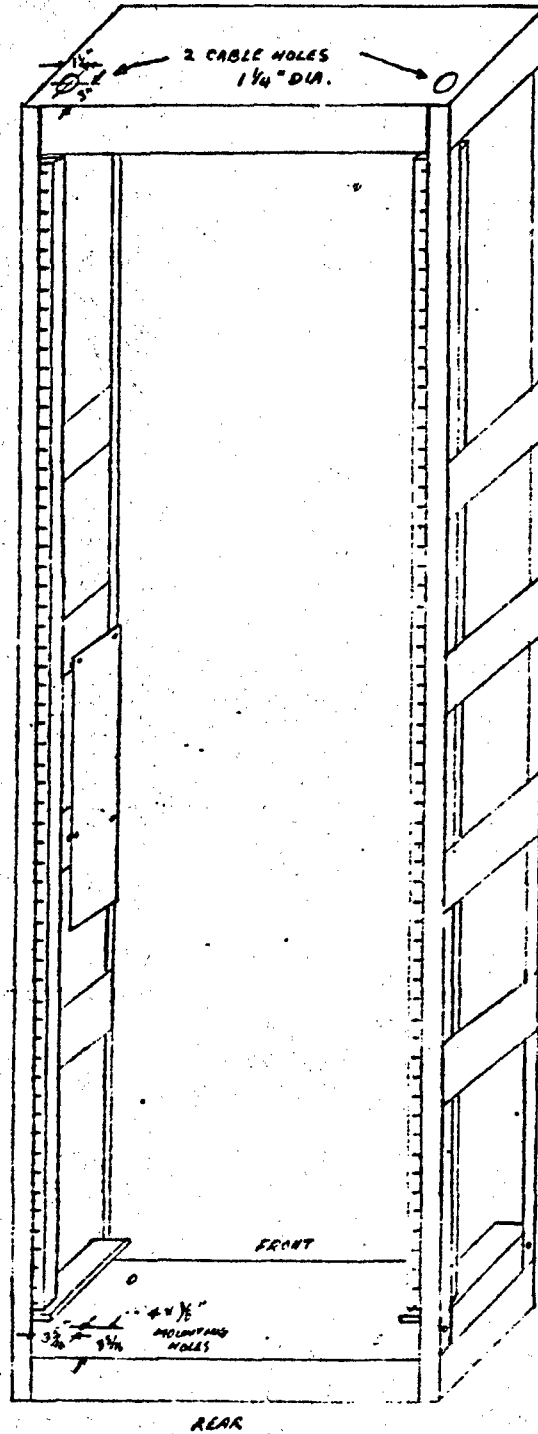
where

$A_1$	=	units of seconds, one
$B_1$	=	" " " , two
$C_1$	=	" " " , four
$D_1$	=	" " " , eight
$A_3$	=	units of minutes, one
$B_3$	=	" " " , two
$C_3$	=	" " " , four
$D_3$	=	" " " , eight

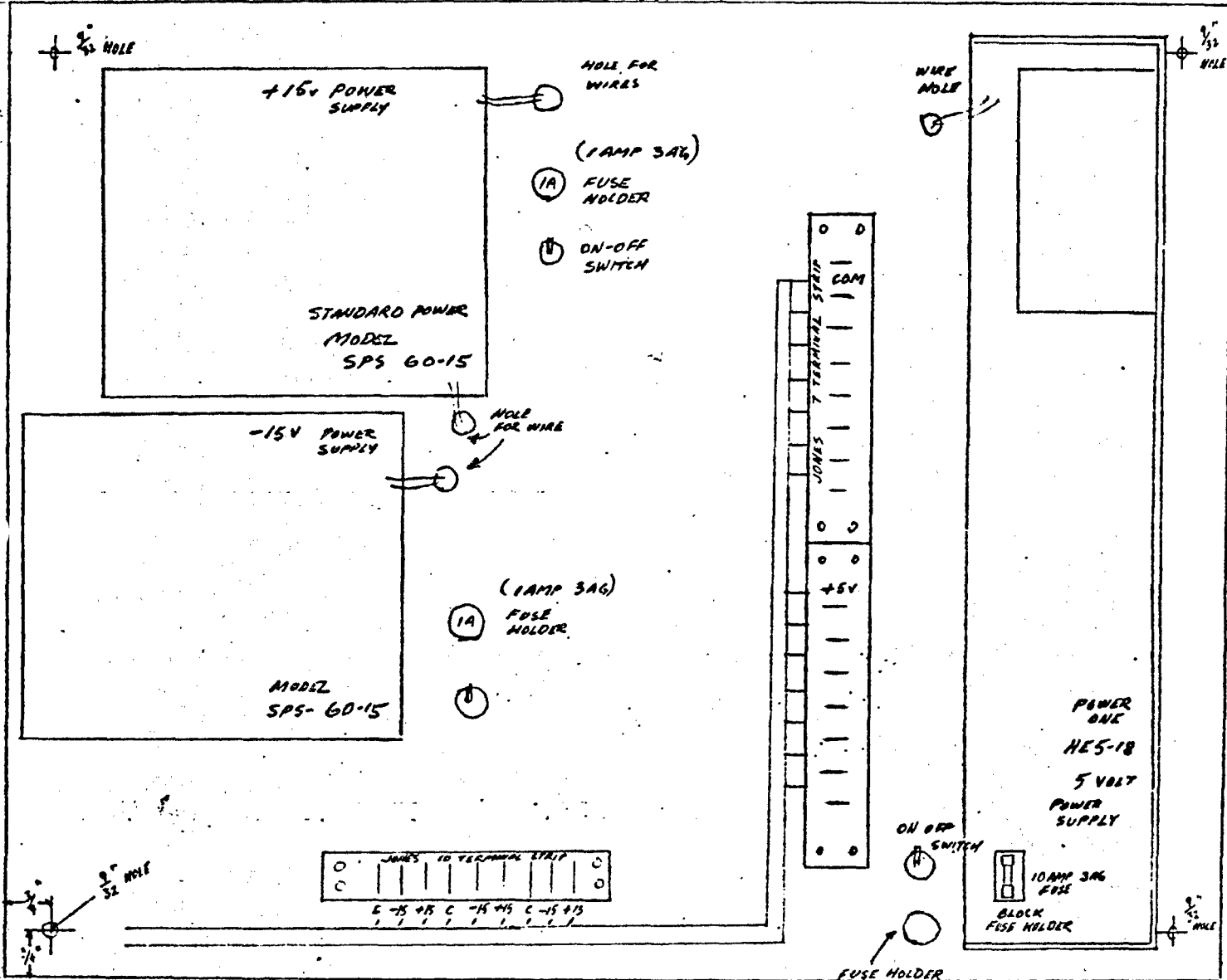
Notice that  $f = 1$  except for  $t = 0.5 \dots 45$  seconds and at ten minute marks at which time  $f = 0$ .

# D, CASCADE BACKPLANE





FRONT TOP VIEW

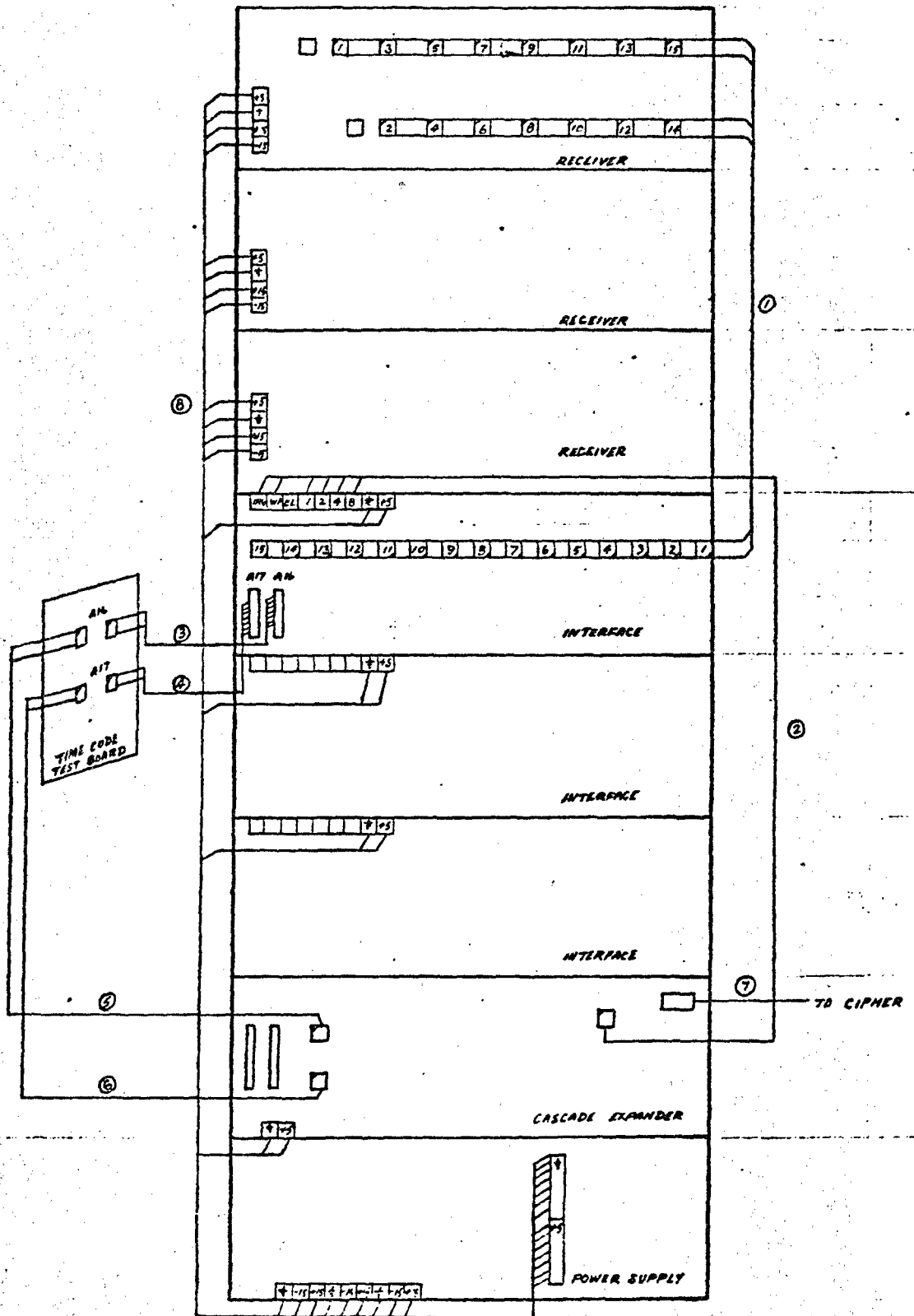


POWER HOOR-UP WIRE USED 14 AWG BELDEN 8916  
 BLACK, RED, WHITE

POWER SUPPLY LAYOUT



SACK VIEW



CASCADE EXPANDER

INTERFACE

B PIN DIP  
SOCKET

1	GREEN	2
2	ORANGE	8
3	GRAY	IRG
4	WHITE	PIN B A19
5		BLANK
6	COAX RG 174	WP
7	YELLOW	4
8	BLUE	1

CABLE 7

CASCADE EXPANDER

CIPHER

16 PIN DIP SOCKET

AMPHENOL 17-20370

1	2	12
2	8	13
3	IRG	8
14	WP	16-17
15	4	15
16	1	14

VIA LOWPASS FILTER 200Ω - .02 MFD CAP.

" " " "

A16

- ① US1    ⑫ US2
- ② US4    ⑬ US0
- ③ TS1    ⑭ TS2
- ④ TS4    ⑮ UMI
- ⑤ UMI2   ⑯ UMI4
- ⑥ UMB    ⑰ TMI
- ⑦ TM2    ⑱ TMI4
- ⑧ UH1    ⑲ UH2

TIME OF DAY  
 TEST POINTS

A	1	
B	2	
C	3	
D	4	
E	5	
F	6	
H	7	
J	8	
⑩ K	9	①
⑪ L	10	②
③ M	11	
④ N	12	⑬
⑤ P	13	⑭
⑥ R	14	⑫
⑪ S	15	
⑩ T	16	⑦
U	17	
V	18	
W	19	
X	20	
⑨ Y	21	⑧
Z	22	

INPUT CONNECTIONS  
 TO TIME CODE BOARD

CABLE 4

(RIBBON ANSLEY 171-16 CABLE)

- ① UH4 ○ UH8
- ② TH1 ○ TH2
- ③ UDI ○ UD2
- ④ UDF ○ UDB
- ⑤ TDI ○ TD2
- ⑥ TDA ○ TDB
- ⑦ HD1 ○ HD2
- ⑧ ○

TIME OF DAY  
TEST POINTS

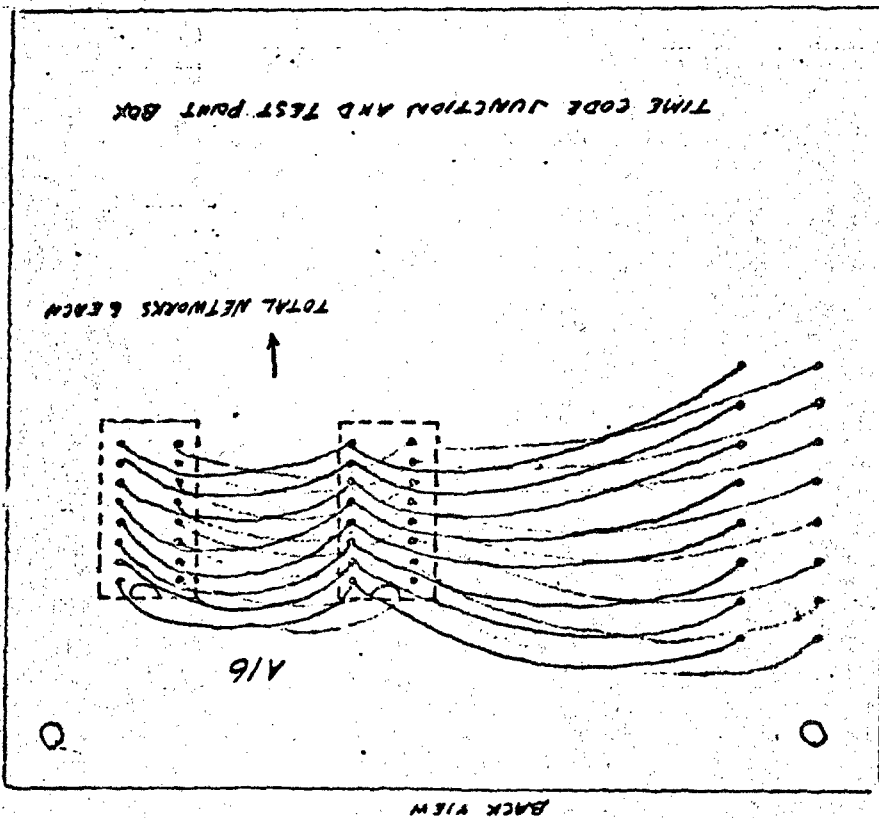
A17

A16

A	1		A	1
B	2		B	2
C	3		C	3
D	4		D	4
E	5		E	5
F	6		F	6
H	7		H	7
J	8		J	8
⑭ K	9	③	K	9
⑬ L	10	④	L	10
⑫ M	11	⑤	M	11 ②
⑪ N	12	⑥	N	12
⑩ P	13	⑦	P	13
R	14		R	14
S	15		S	15 ⑬
T	16		T	16
U	17		U	17
V	18		V	18
W	19		W	19
X	20		X	20
Y	21		Y	21
Z	22		Z	⑯ 22 ⑰

INPUT CONNECTIONS  
TO TIME CODE AND  
DAY TIME CODE BOARD

1. BOARD VECTOR 16P44-062 17" x 4 1/4" WIRE REQUIRED 12 EACH
2. 16 PIN WIRE WRAP DIP SOCKETS ROBINSON AUGMENT 17-163-WB WIRE REQUIRED 50 FT.
3. ALPHA WIRE 5952 #28 SOLID WIRE REQUIRED 50 FT.
4. USECO TERMINALS #2003B1 REQUIRES .065 DIA M7G WOLE
5. TERMINALS REQUIRED 108 EACH



## F. Problems Encountered and Some Suggested System Improvements

The digital system has, in general, proven to be a reliable method of accurately transmitting low frequency data. Some problems which potential users should be aware of have been encountered in the operation of the system. These are discussed below along with certain design improvements which should be considered for upgrading reliability and overall system performance.

In this appendix potential and actual problems are divided into two categories. Firstly there are those that require major modifications, and secondly those which are considered minor and are correctable by changes on a single printed circuit board.

### Potential Problems

#### A. Time ambiguity

For low frequency data rate measurements (tilt, strain, telluric, creep etc) for which the system is presently being used, timing accuracy better than  $\pm 10$  minutes was not necessary. Since this is the case efficient use of phone line channels was possible by multiplexing data randomly to a receiver approximately once every 10 minutes. Shorter period data are obtained from an on site analog recorder. For applications where higher digital data rates are required, transmit and dumping times can be decreased to a lower limit of about one sample every 80 seconds  $\pm 20$  seconds. At this rate tape useage will be much greater.

#### B. Digital Data Turn around

Although analog data is available within 10 minutes of the field measurement with the present system, the closest approach to "real time" accessibility of the digital data is about 2 hours. This results from the use of an incremental digital tape recorder from which the data is transferred to a C.D.C. 7600 computer. The use of a minicomputer (e.g. P.D.P.11) with access to the 7600 could reduce this time if it became necessary to have digital data turn around

of much less than this.

### Actual Problems

#### A. Reed Relays

Two years of operating experience have shown that the reed relay is the single most failure prone element in the system. This has proven to be very serious for transmitters in isolated locations. A design modification to avoid this problem involving the use of solid state switches has been lab tested with good initial results. This modification replaces all 16 reed relays with a single 16 channel CMOS analog multiplexer-decoder I.C. The transmitter multiplexer board circuit diagram with the modification for solid state switching is shown below.

The cost of one solid state multiplexer is about 1/2 the cost of the reed relays. Quality control on the relays is also poor, so replacement by the Harris I.C. (HI-506A) would eliminate the present need to individually test each relay before assembly. In the past up to 5% of batches delivered were defective.

#### B. Channel tracking

In the present system an open channel can be caused by not only a broken wire but also by a defective relay. This has proven to be a common problem and results in the open channel tracking the previously transmitted channel. This false data looks real and is not easily or automatically detected. The use of the solid state multiplexer discussed in the previous section would also almost eliminate this problem.

#### C. Battery Voltage\*

Due to the high current drain during transmissions, the nominal 5 volt air cell voltage can be pulled down below the minimum operating voltage on some I.C. packages in the transmitter. This can result in channel skipping. To avoid

\*after suggestion by Sam Rodriguez





this condition, battery voltage during transmission should always be kept above 4.9v.

#### D. Latch-Up

Occasionally transmitters will not power down after power-up. This condition is serious since it leaves a tone on the line that does not make it possible to receive data from other stations sharing the same phone line channel. This situation could be avoided with a fail-safe power down circuit. Since only one JK flip-flop in IC-5 is used, the other could be connected as a one-shot with a pulse width of several seconds. If power was still on after this time period, the one-shot would provide a pulse to the off-selection input shutting down power and removing the tone from the channel.

#### E. Receiver Sensitivity

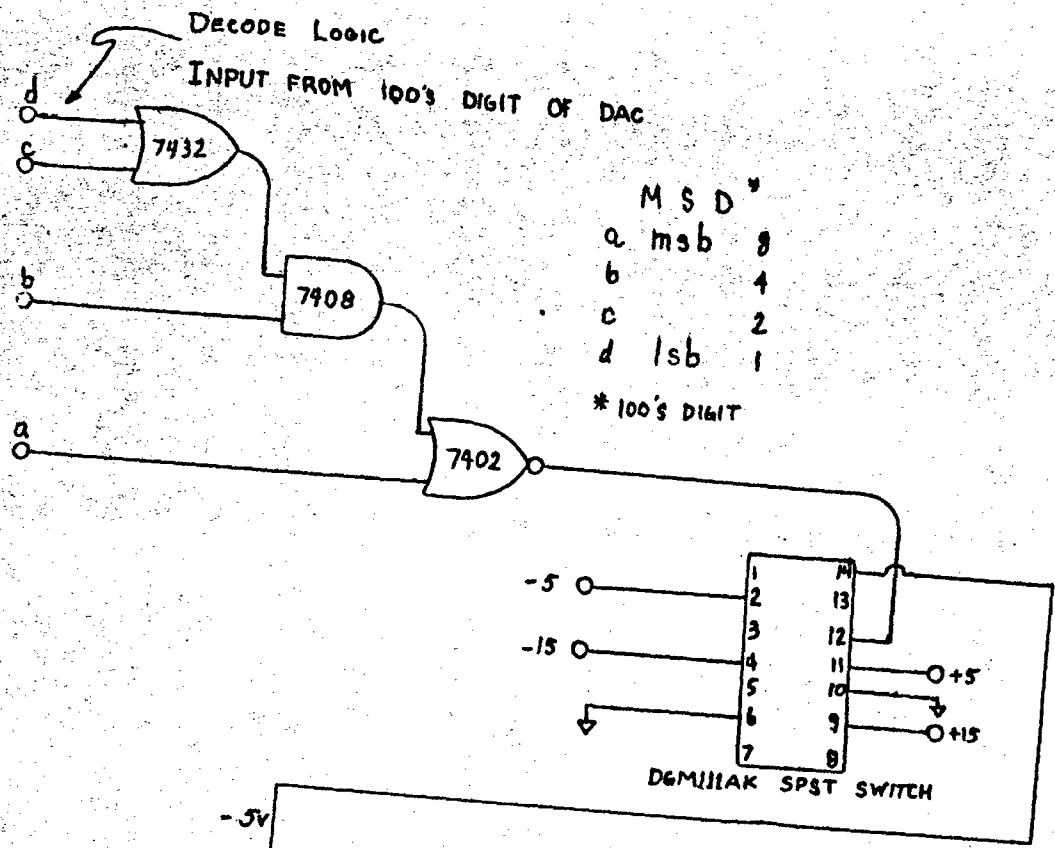
In the present receiver design, the least two significant digits are used to generate an analog record. For many sensors this implied a gain that is too high and results in chart recordings that are difficult to read. Use of a 3 digit D.A.C. (i.e. a factor of ten down in gain) can generate records for which the gain is too low. A compromise between the two possibilities presently used can be realized in the circuit shown below. A prototype is currently being, tested with good initial results. Here a 3 digit DAC is used, and coded such that the output voltage per digit is twice that of a straight 3 digit conversion.

#### F. Phone line input\*

The digital transmitter output is a FSK tone with a low duty cycle. The phone line or radio input should be measured and set with the transmitter on even though normally this signal is not present. This is necessary since the composite signal is of higher level than the single carrier.

#### G. Old data flag

In the current interface design there is a provision for flagging old or bad data samples that is presently not used since a system for detecting these data has not been designed. If a station stops transmitting, therefore, the last  
\*suggested by John Van Schaack



INPUT - OUTPUT CHARACTERISTICS  
(X = DON'T CARE)

INPUT COUNTS	OUTPUT VOLTAGE
X 0 0 0	0 . 0 0
X 0 0 1	0 . 0 2
X 0 1 0	0 . 2 0
X 1 0 0	2 . 0 0
X 2 0 0	4 . 0 0
X 4 0 0	8 . 0 0
X 4 9 9	~ 1 0 . 0 0
X 5 0 0	0 . 0 0
X 5 0 1	0 . 0 2
X 5 1 0	0 . 2 0
X 6 0 0	2 . 0 0
X 9 0 0	8 . 0 0
X 9 9 9	~ 1 0 . 0 0

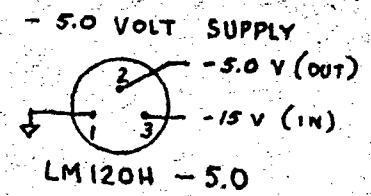
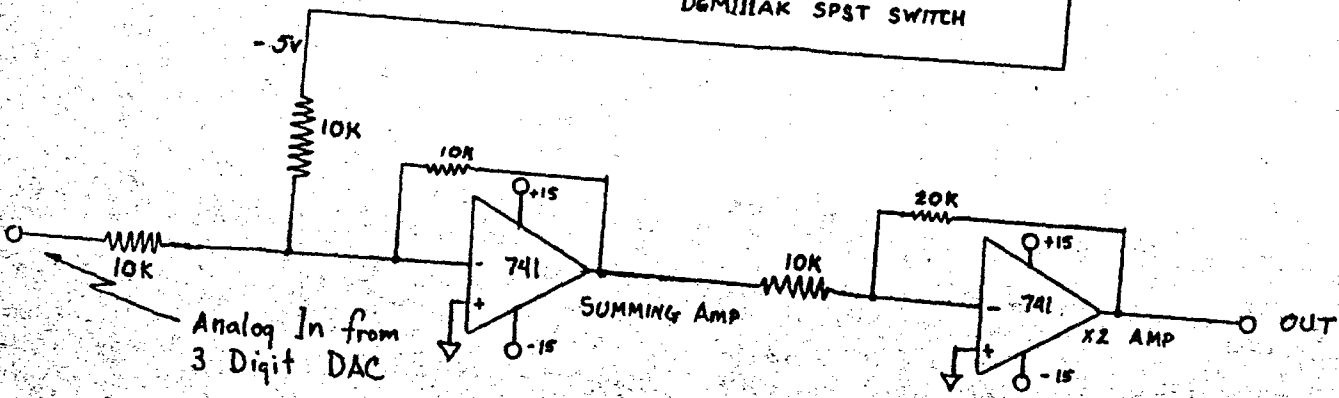
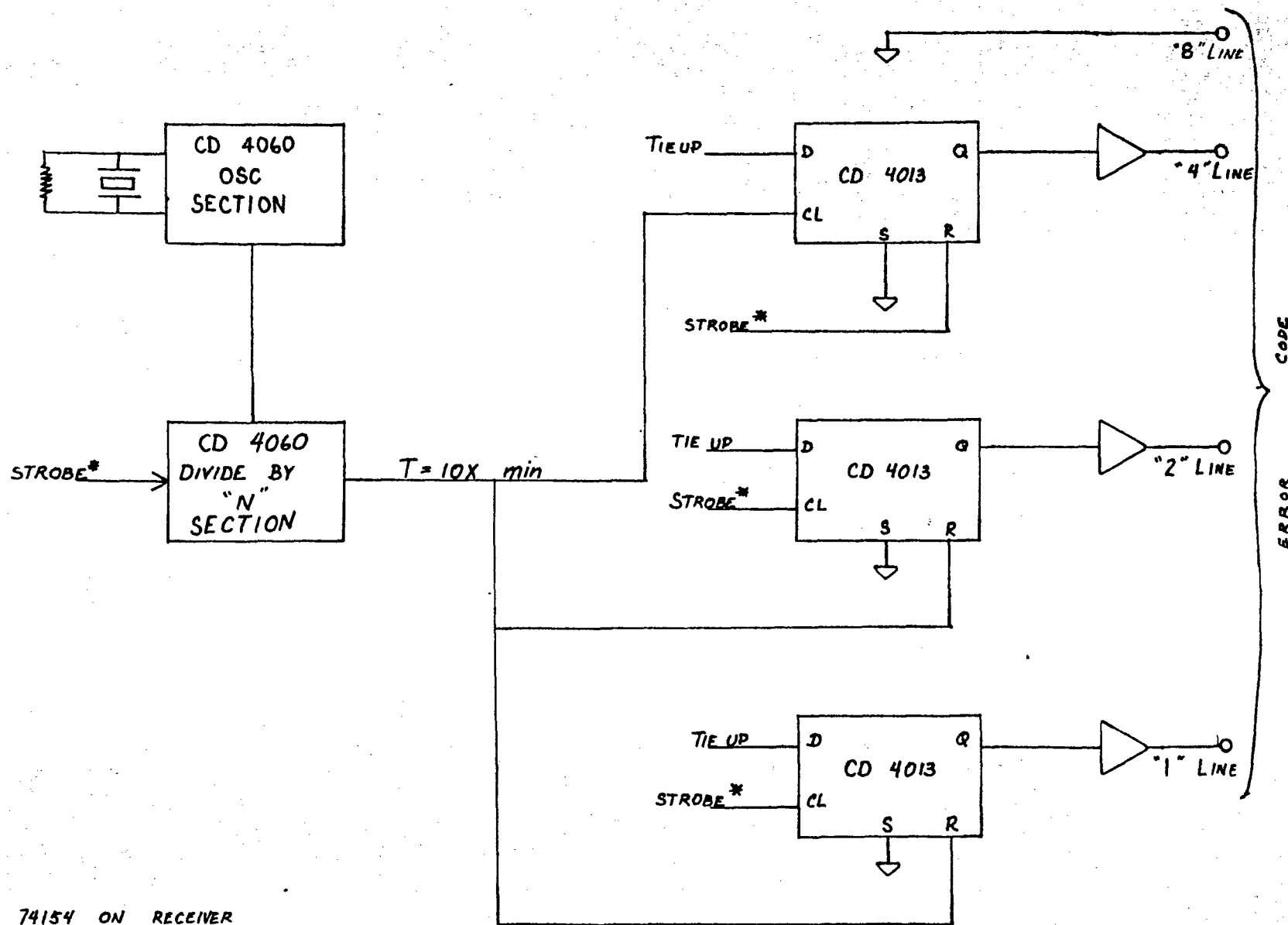


CHART RECORDER BIAS STEPPER

transmission will be stored indefinitely in the latch. One possible detection circuit for identifying old data is shown below. Operation is as follows: The oscillator-divider generates a pulse train with a period of 10X minutes. If a strobe from the receiver-decoder does not reset the divider within 10X minutes the divider output sets one D-type flip-flop and resets two others in order to change the error flag input on the interface from binary 3 (no flag) to binary 4 (flag).



\* FROM 74154 ON RECEIVER

TYPICAL CHANNEL

OLD DATA FLAGGING CIRCUIT