UNITED STATES
DEPARTMENT OF THE INTERIOR
GEOLOGICAL SURVEY

Office of Earthquake Studies
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A CODE GENERATING SELF-CALIBRATING SEISMIC AMPLIFIER

by

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(with CRYSTAL VCO CENTER FREQUENCY STABILIZER by E. Gray Jensen)

Open-File Report 80-387

INTRODUCTION

The original self-calibrating seismic amplifier system described by Van Schaack (1975) has been modified to accommodate an 11 bit code generating calibrator. The code allows positive visual or computer identification of individual seismic data channels. In addition to the circuit and layout modifications, two electronic tests related to the selection procedures of integrated circuits for the VCO section are described.

A center frequency stability problem with the original preamp/VCO design has been corrected by a crystal VCO center frequency stabilizer circuit described by Jensen (1977), and included in this report.

J302M PREAMPLIFIER AND VOLTAGE-CONTROLLED OSCILLATOR UNIT

A. General

The J302M Preamplifier and Voltage Controlled Oscillator (VCO) Unit is designed primarily as a seismic signal amplifier and conditioner. This unit amplifies and filters seismic signals in the microvolt to millivolt range and bandwidth or from 0.1 to 30 Hz (Fig. 2), then frequency-modulates an audio carrier with the amplified seismic signal. This method allows low-frequency seismic signals to be telemetered by telephone line or by radio link to a recording site. The modulated carriers can be multiplexed so that as many as 8 seismic signals can be transmitted over one voice-grade phone line or radio link.

B. Specifications

1. Noise referred to input: 1.0 microvolt peak-to-peak with a source impedance of 10,000 ohms and a bandwidth of 0.1 Hz to 30 Hz.
2. Bandwidth, 3 db points: 0.1 Hz to 30 Hz with 12 db/octave rolloff.
3. Gain: Voltage gain 90 db max, with 48 db atten in 6 db steps.
4. Input: Differential, 10,000 ohms input impedance.
5. Supply voltage: $\pm$4.05 vdc at 200 microamps with output level at -10 dbm.
6. VCO stability:* 100 ppm/degree centigrade, without stabilization.

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*Before compensation.

7. Output distortion: Harmonic frequencies less than 3% of fundamental frequencies.
8. Output level: -5 dbm maximum into a 600 ohms load, adjustable.
9. Output impedance: 600 ohms.
10. Carrier deviation: ±125 Hz, limited to 135 Hz maximum.
11. VCO sensitivity: Adjustable from $\frac{2\text{Hz}}{\text{microvolt}}$ to $\frac{0.001\text{ Hz}}{\text{microvolt}}$ referred to input.
12. Operating temperature range: -30 degrees C to +50 degrees C.

C. Theory of Operation

The J302M (Fig. 1) consists of a preamplifier (A1), an amplifier (A2), and a voltage-controlled oscillator (VCO), along with associated filtering and wave-shaping circuitry. The seismic signal is direct-coupled to the preamplifier which has an input impedance of 10,000 ohms. This amplifier stage has resistance and capacitance feedback to provide a fixed gain of 48 db and low-pass filtering with 6 db per octave rolloff above 30 Hz. The D.C. offset of this amplifier can be nulled with R7.

The preamplifier and amplifier stages are resistance-capacitance coupled through C3 and R8, resulting in high-pass filtering with 6 db per octave rolloff below 0.1 Hz. Series resistors R25 through R33 provide 48 db of attenuation in 6 db steps.

The amplifier stage also has resistance and capacitance feedback with a fixed gain of 42 db and low-pass filtering with 6 db per octave rolloff above 30 Hz. The D.C. offset of this stage can be nulled with R13.

Both A1 and A2 are micropowered integrated circuit operational amplifiers that require about 15 microamp each to operate at ±4 VDC.

The output of the amplifier stage is resistance-capacitance coupled through C5 and R14 and R15 to the VCO stage to produce 6 db per octave rolloff below 0.1 Hz. The result is an amplifier system with a maximum voltage gain of 90 db and a bandpass of 0.1 Hz to 30 Hz with 12 db per octave rolloff outside of these frequencies.

The VCO utilizes only the VCO section of a COS MOS phase-locked-loop integrated circuit. The amplified seismic signal is fed into the VCO through potentiometer R15, which functions as a deviation control. The center frequency of the VCO is determined by C6 and R22 with potentiometer R21 being a fine adjustment control for the center frequency. The center frequency of the VCO is temperature compensated by the circuit consisting of R17, R18, R19, and thermistor R20. The output of the VCO is fed through potentiometer R23, the output level adjust control, into I1, C8, and C7, the wave-shaping network, then into the output transformer T1. The center frequencies given in Table 1 have become standard in the transmission of seismic data by constant bandwidth methods. All frequencies are operated in a constant bandwidth system, each having a maximum deviation of ± 125 Hz.

D. Alinement Procedures

1. Amplifier section

Insert integrated circuits A1, A2, and VCO into their respective sockets (Fig. 3), shunt the preamplifier input with a 10 K ohm

resistor, and apply ±4 VDC power. Connect an oscilloscope to common and tie point 1 (TP1) and adjust R7 for OVDC ± 5 MV. Next, connect the oscilloscope to tie point 2 (TP2) and adjust R13 for OVDC ±5 MV. Lastly, connect the oscilloscope to the amplifier monitor and remove the 10 K ohm shunt from the input to A1. Connect a microvolt AC signal source across the inputs to A1 and monitor the amplifier output for proper gain at each attenuator setting. Gains may vary a maximum of 10%.

2. VCO section

To align the VCO to the proper center frequency, determine the resistor and capacitor values from Table 1 and install them. These values are only approximate and some trimming may be required. R21, the center frequency adjust pot, provides about 2% adjustment of the center frequency.

Load the secondary of output transformer T1 with 600 ohms and connect a frequency counter and an oscilloscope across the load. Set the attenuator switch to 48 db so that no amplifier noise will modulate the carrier frequency. C7 should be trimmed to obtain a maximum output with distortion held to less than 3%. C8 may be trimmed if necessary to meet this objective.

To set the deviation of the VCO, apply 3 VDC between common and the amplifier monitor, and adjust R15 for 125 Hz offset of the carrier frequency. Reverse the polarity of the 3 VDC and check for 125 Hz in the opposite direction. A positive monitor voltage should give a positive deviation.

For a more precise setting of the carrier deviation to standardize the overall gain between units in hertz/microvolt, the following procedure can be used: With the attenuator set at 0 db, apply a 10 microvolt RMS 5 Hz signal to the preamplifier input. Measure the amplifier output at the amplifier monitor in volts peak-to-peak. Insert the measured value in the following equation. The result will be the proper sensitivity of the VCO in hertz/volt:

$$\frac{36.9}{\text{measured volts peak-to-peak}} = \text{deviation in hertz/volt}$$

Apply a known dc voltage of 3 volts or less to the amplifier monitor and set the deviation control (R15) for the proper number of hertz offset. The preamplifier/VCO sensitivity at this setting is 1.32 Hz/microvolt referred to the preamplifier input.

E. Tests

1. VCO chip voltage-frequency stability tests

A small number of VCO chips are very sensitive to supply voltage changes wherein the frequency of the VCO may change as much as 50 Hz per KHz center frequency with a 1% change in supply voltage. The acceptable level of change is 5 Hz per KHz with a 1% change in supply voltage. The following screening test can be used to find acceptable VCO chips.

Install a VCO chip in its socket, connect the battery supply and read the VCO frequency. Disconnect one side of the

battery supply voltage, insert a germanium diode in series and reconnect the battery. Read the VCO frequency and measure the voltage drop across the diode. Find the Hz per KHz change of the VCO frequency with the change in the supply voltage. Divide this by the % change in the supply voltage. The answer will be the Hz per KHz change in frequency with a 1% change in supply voltage. It is good practice to use the VCO chips that are least sensitive to supply voltage change in the higher frequency units.

2. Temperature compensation tests

Individual VCO chips should be tested in circuit.

The temperature compensating circuit consists of R17, R18, R19, and R20. Changing the value of R19 will change the amount of temperature compensation provided the VCO chip. The nominal value of R19 is 30k ohms but can vary between 22k ohms and 47k ohms for acceptable VCO chips.

The VCO center frequency should be measured at room temperature and again at a lower temperature. The freezer section of a refrigerator or deep freeze is adequate. It is not necessary to know the exact temperature but the difference should be 40 to 70 degrees F. If the VCO varies by more than 5 Hz from center frequency with a 40 degree F change in temperature, R19 should be changed. To find the correst resistor value, the following procedure should be used:

Replace R19 with a resistor substitution box that has values from 22k ohms to 47k ohms. At room temperature, connect a frequency counter to the VCO and record the frequency at each resistor value from 22k ohms to 47k ohms. Place the VCO in the cold environment and wait 30 minutes. During the tests there should be no air blowing on the VCO. Again measure and record the VCO frequency at each resistor value from 22k ohms to 47k ohms. The resistor value that results in the smallest change between the two frequency readings at the different temperatures should be installed in the circuit. If the VCO frequency can not be overcompensated within the range of 22k ohms to 47k ohms, the chip should be replaced and a new chip installed. The tests should be repeated on the new chip.

Table 1: Frequency Dependent Components

Frequency	C6 uf	C7 uf	C8 uf	L1	R34 (ohms)
680 Hz	.0015	.018	.01	ML-6	300
1020 Hz	.0015	.01	.082	ML-6	270
1360 Hz	.001	.015	.0082	MOT	240
1700 Hz	.001	.0068	.0050	MOT	200
2040 Hz	.001	.0047	.0039	MOT	180
2380 Hz	.001	.0056	.0033	ML-3	150
2720 Hz	.00068	.0047	.0027	ML-3	130
3060 Hz	.00068	.0039	.0022	ML-3	100

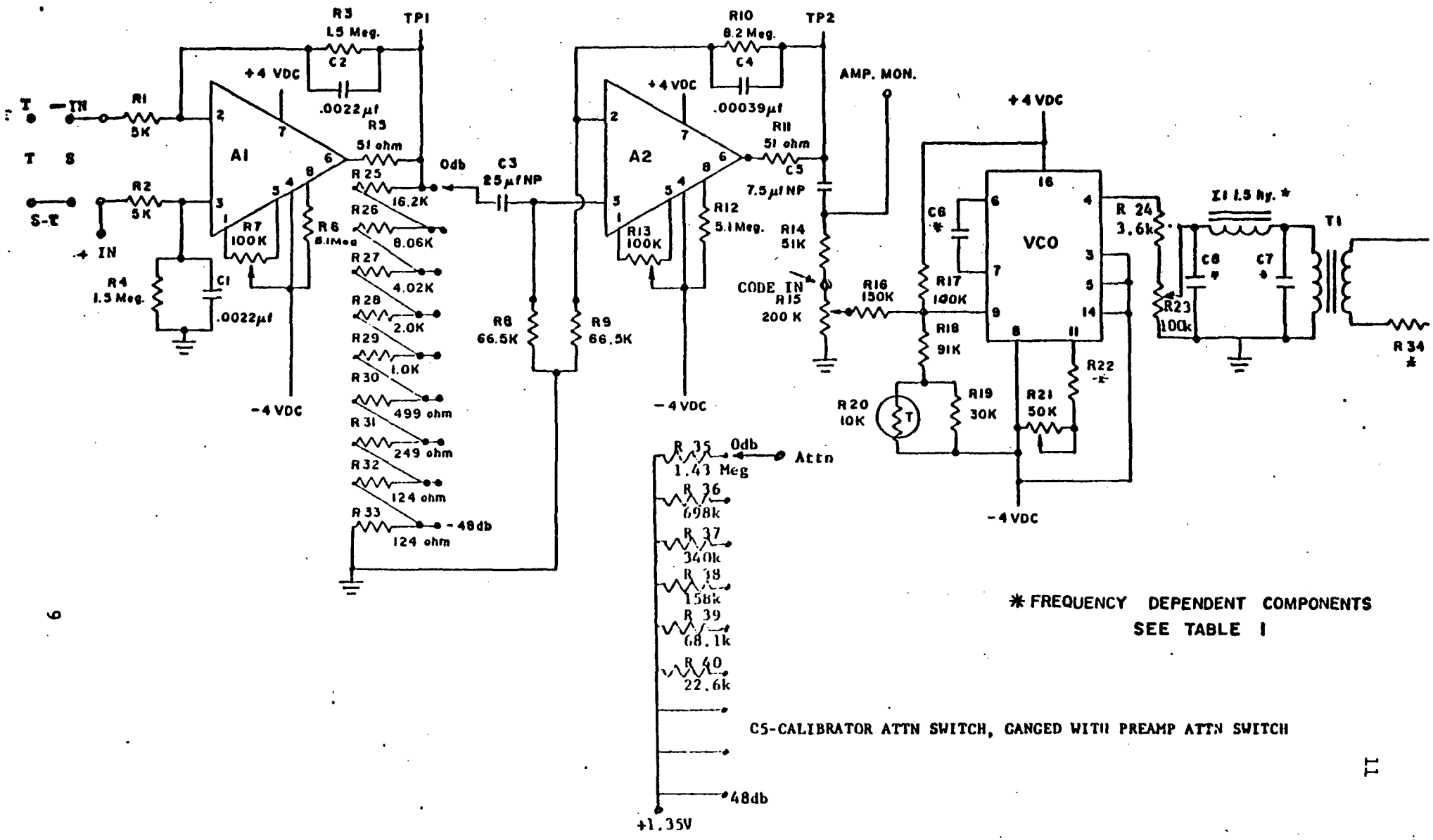
R22 varies with individual VCO IC's. Minimum value for R22 should not be less than 240 K ohms. Maximum value may be 3 Meg ohms.

Table 2: J302M Preamp/VCO Parts List

1,C2	Capacitor .0022 uf	Aerovox CK05BX222K
C3	Capacitor 25 uf 6VNP	GE 29F538
C4	Capacitor .00039 uf	Aerovox CK05BX391K.
C5	Capacitor 7.5 uf 6VNP	Sprague 151D755X9006X2
C6	Capacitor .00068-.0015 uf	Aerovox 3419-100A series
C7,C8	Capacitor .0027-.003 uf	CD WMF Series (frequency dependent)
R1,R2	Resistor 4.99k ohm	RN55D 1%
R3,R4	Resistor 1.50 meg ohm	A-B type CC 1%
R5,R11	Resistor 51 ohm	1/4W 5%
R6,R12	Resistor 5.1 meg ohm	1/4W 5%
R7-R13,R23	Resistor 100k ohm Pot	Spectrol 43W104
R8,R9	Resistor 66.5k ohm	RN55D 1%
R10	Resistor 8.25 meg ohm	A-B type CC 1%
R14	Resistor 51K ohm	1/4W 5%
R15	Resistor 200k ohm Pot	Spectrol 43W204
R16	Resistor 150k ohm	1/4W 5%
R17	Resistor 100k ohm	1/4W 5%
R18	Resistor 91k ohm	1/4W 5%
R19	Resistor 30k ohm	1/4W 5% nominal (varies w/VCO chip)
R20	Thermister 10k ohm	Fenwal KP41J2
R21	Resistor 50k ohm Pot	Spectrol 43W502
R22,R34	Resistor	1/4W 5% Frequency dependent
R24	Resistor 3.6k ohm	1/4W 5%
R25	Resistor 16.2k ohm	RN55D 1%
R26	Resistor 8.06k ohm	RN55D 1%
R27	Resistor 4.02k ohm	RN55D 1%
R28	Resistor 2.00k ohm	RN55D 1%
R29	Resistor 1.00k ohm	RN55D 1%
R30	Resistor 499 ohm	RN55D 1%
R31	Resistor 249 ohm	RN55D 1%
R32,R33	Resistor 124 ohm	RN55D 1%
R35*	Resistor 1.43 meg ohm	A-B type CC 1%
R36*	Resistor 698k ohm	A-B type CC 1%
R37*	Resistor 340k ohm	RN55D 1%
R38*	Resistor 158k ohm	RN55D 1%
R39*	Resistor 68.1k ohm	RN55D 1%
R40*	Resistor 22.6k ohm	RN55D 1%
L1	Inducto 0.7 Hy	UTC/TRW ML-3
	Inductor 4 Hy	UTC/TRW ML-6
	Inductor 1.5 Hy	Motorola 25B82751D01
T1	Transformer	UTS/TRW S -14
A1,A2	Micropower Op Amp	National LM4250CN
VCO	C MOS Phase lock loop	RCA CD4046AE
SW1	Switch, 12 position 2 pole	Grayhill 71ASF30-02-1-12S-C
S1,S2	Socket, 16 pin DIP	Amphenol 821-25011-164
	Battery, 4 ea 4.05 V	Mallory TR233R
	Diodes 4 ea	IN34A in series with batteries
	Terminals 23 ea	USECO 2003B
	Connector, Power 3 pin	W.S. Deans 3 pin pair
R-S, R-T	Resistors, 1/4 W 5%	Seismometer damping resistors matched With individual seismometers.

*Indicates components used in the calibrator circuit.

Figure 1. J302M Preamplifier / Voltage Controlled Oscillator



* FREQUENCY DEPENDENT COMPONENTS
SEE TABLE I

C5-CALIBRATOR ATTN SWITCH, GANGED WITH PREAMP ATTN SWITCH

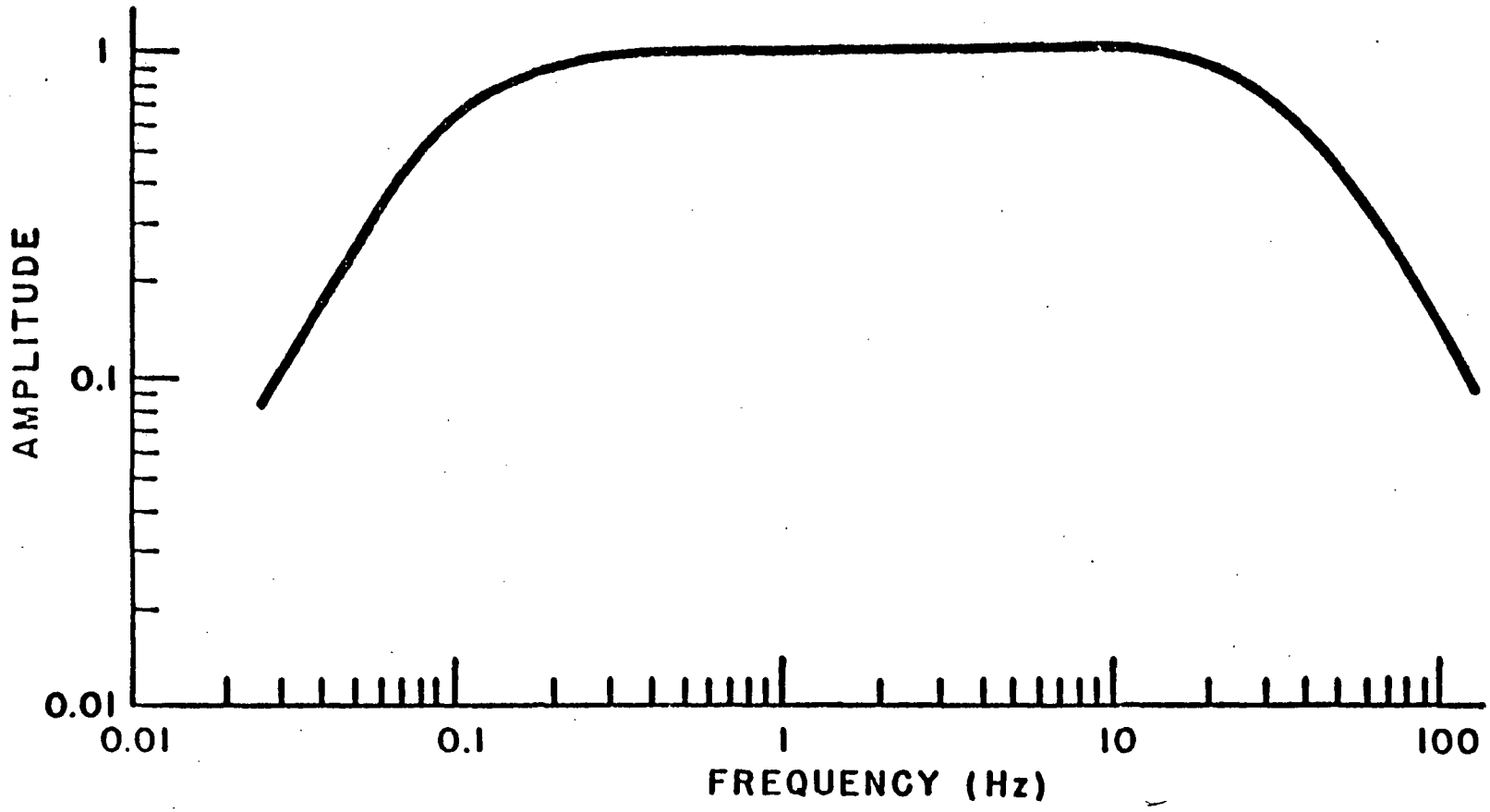
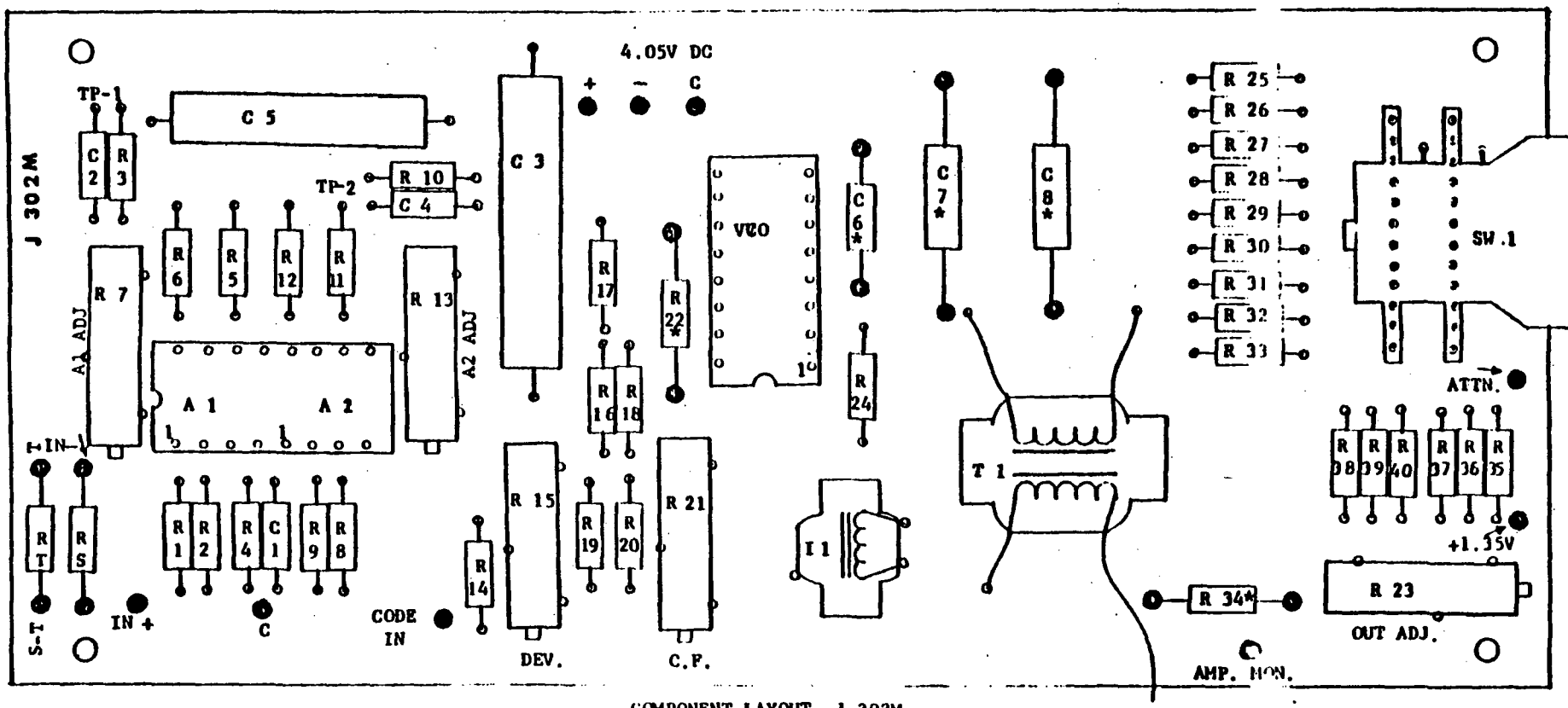
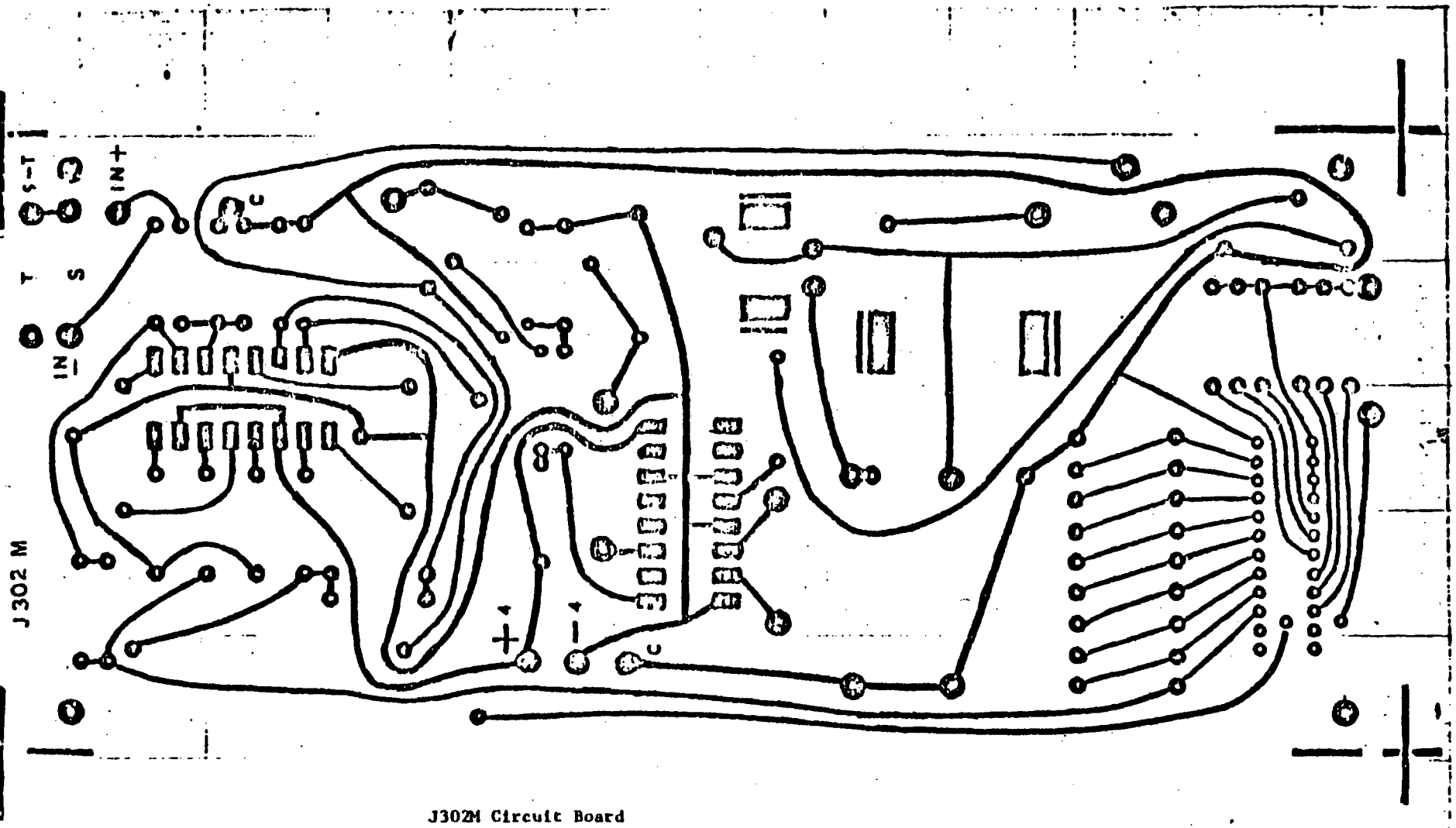


Figure 2. Frequency response of J302 Preamplifier/VCO at amplifier monitor.



COMPONENT LAYOUT, J 302M

Figure 3



J302M Circuit Board

Figure 4

J302M Preamp/VCO - C5 Calibrator

Interconnection Diagram

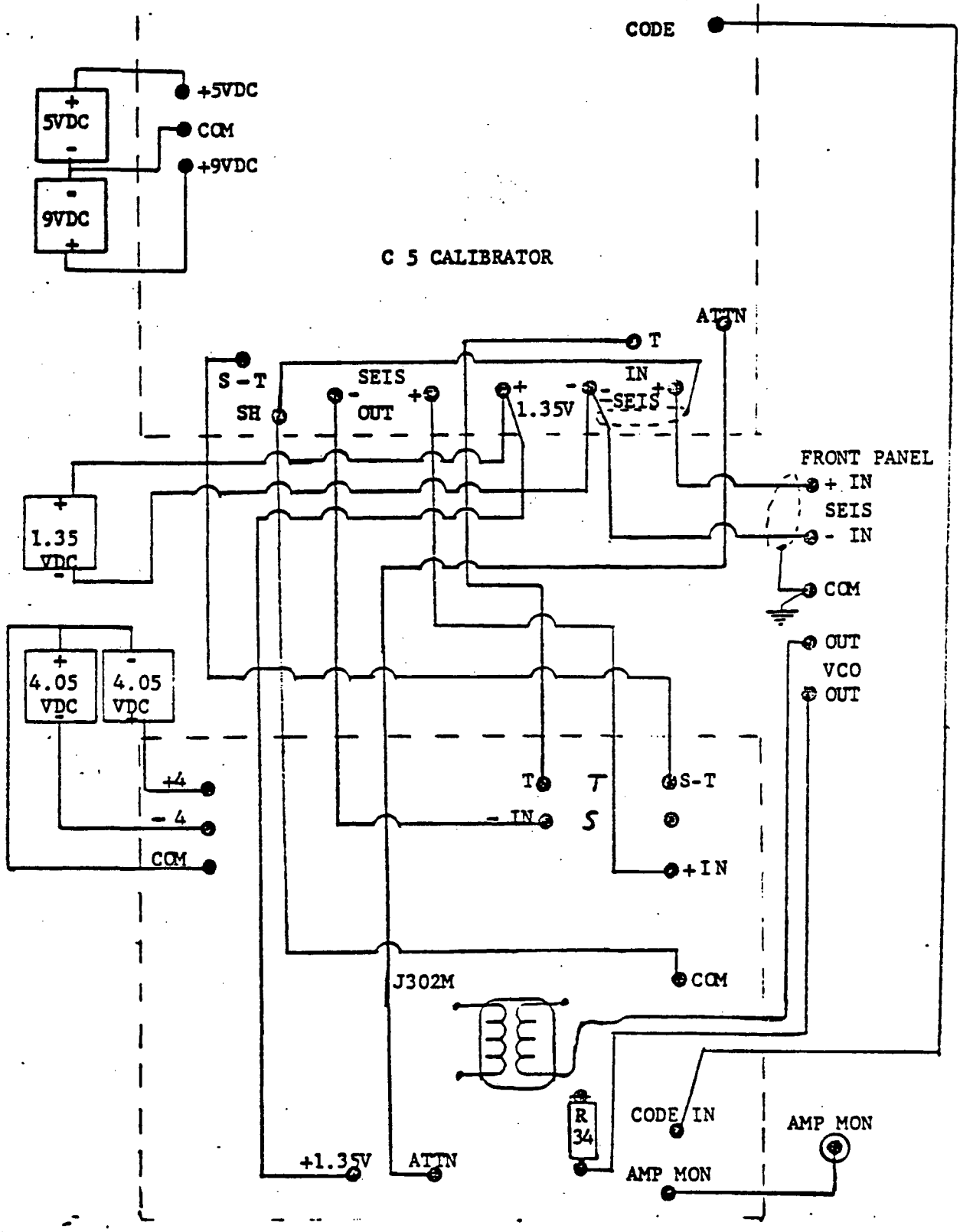


Figure 5

C5 CALIBRATOR

The C-5 Calibrator is a modification of the C-4 Calibrator described by J. Van Schaack in an earlier paper. The C-5 Calibrator includes a code-generating circuit used to produce an identification code for each unit. The calibrator applies a mass release test to the seismometer and a D.C. step test to the preamp/VCO. The clock and relay control circuit is the same as for the C-4 except for minor changes in resistor and capacitor values controlling the duration of individual phases of the calibration test. The test signal generation circuit, Figure 1a, has been modified to overcome real or theoretical deficiencies encountered in the C4 calibrator. The sequence, timing, and results of the tests applied are illustrated in Figure 1b. The attenuator resistors used in the calibrator are mounted on the J302M preamp/VCO and are controlled by the front panel attenuator switch on the J302M. The S and T seismometer damping resistors are also located on the J302M near the preamp input. The power for the identification code is supplied by the 9 VDC battery used to operate the relays. The power for the code section is supplied through relay 4 which is activated only during the first 5.27 seconds of each calibrating sequence.

A. Operation

Once each day the calibrator applies a known direct current step to the seismometer coil, releases it, then applies a DC voltage step to the input of the amplifier-VCO.

The frequency response of the system can be calculated from a digitized signal. Simple inspection of the Develocorder trace, however, will indicate polarity reversals in the telemetry, recording, and playback systems after stations have been installed and checked out and any gross changes in seismometer sensitivity or natural period can be detected by comparison with previous traces. "Dead" times in the calibration sequence will give a measure of the electronic noise of the system.

The clock portion (Fig. 4) provides a square wave output with one negative edge per day, which triggers sequentially a chain of 3 one-shot multivibrators (Fig. 2), the first two having periods of about 8 seconds each and the third having a period of 20 seconds. Multivibrator 1 closes relays 1A and 1B (Fig. 1B), which applies a current to the seismometer and simultaneously terminates the amplifier with 698 ohms, and turns on code generation circuit. The 8-second closure time allows the mass to stop oscillating. About 3 milliseconds before relays 1A and 1B are released, relay 2 is closed to insert a 24 db pad. This pad attenuates the seismic background noise, resulting in an improved signal-to-noise ratio for the seismometer release test. Eight seconds later, relay 2 returns to normal and relay 3 is closed to apply a step voltage to the input of the amplifier-VCO. After 20 seconds, relay 3 will return to normal operation for another 24 hours.

B. Power Supplies

Mercury batteries are used as a standard (1.35 volts) in the seismometer circuit and to power (5.4 volts) the clock and multivibrator

circuits. These batteries are used mainly because of their high capacity and their stable voltage. Quiescent current drain is about 250 microamps. (Short pins 14, 13, 6, 9 of CD4001 to minimize current drain.) Even in extremely cold temperatures, the mercury batteries provide enough power to operate the clock and multivibrator circuits for one year. A 9 volt alkaline transistor battery, used to close the relays, has both adequate shelf life and capacity to provide power for a year. Only fresh battery replacements should be used.

C. Testing

Check out procedure:

1. Clock. The oscillator frequency can be adjusted with C_1 (Fig. 4) and monitoring pin 15 of the CD4045AE chip, using a 25 pf capacitor in series with a scope probe to minimize loading effects of scope and frequency counter. Adjust C_1 for a reading of 397.662 KHz; if unable to adjust this low, add a 25 pf capacitor parallel to C_2 and adjust C_1 for a reading of 397.669 KHz. Frequency is adjusted low to compensate 9 Hz for loading and 4 Hz to compensate for room temperature to 50 degrees F. The crystal is not temperature-compensated; stability is approximately 1.5 ppm/^0C.

2. Trigger test. Connect the seismometer to the proper terminals and make sure S and T resistors are in place. Switch VCO attenuator switch to 36 db position. Two separate grounds are necessary: the seismometer cable shield, and the ground for relay control and VCO. All tests are made using an alined VCO and with respect to ground.

Monitor-code in on VCO with scope or recorder. Using a clock monitor circuit (Fig. A) connect ground and one red lead to clock (CK) (Figs. 4 and 5) and observe led indication when clock is high for 5.27 seconds. While clock is high, connect the other red lead to trigger (T-Figs. 5 and 2). When the clock goes low, the timing sequence of the relay control circuit is started. Disconnect red lead on trigger while clock is low to avoid retriggering.

3. Code generation. The CD4001 receives both lows (Clock and IC3) and energizes relay 4 applying power to the code circuit (Fig. 3). Initially there is a one-second trigger delay provided to the CD 4021 by R26 and C13. Half of the CD4011 is an oscillator which determines the pulse width of the code pulses. There should be 3.35 to 3.5 seconds from the leading edge of the tenth pulse. Substitute values for R30 to obtain 10 positive transitions in the time above. The serial output code "ones" are approximately 0.5V and "zeros" approximately 0.3V. There should be 11 pulses when time is set properly. Power is removed when clock goes high again.

4. Relay control circuit. The relay control circuit consists of a CD4049AE hex inverter which triggers sequentially a chain of 3 one-shot multivibrators, each of which an RC time constant determines the length of time a relay is energized (Figs. 1B and 2). Relay 1A and 1B should be energized 8.5 seconds min--10.05 seconds max (C4 and R6). Relay 2 should be energized 8 to 12 seconds (C6 and R8). Relay 3 should be energized 18 to 22 seconds (C8 and R15). Necessary changes should be made in above resistors to get proper timing.

5. Reset - The C5 calibrator once a day applies a calibration and tests the seismic package by utilizing a CD4020AE chip which can be reset by applying a positive voltage (Fig. 4). At this time the CD4020AE will start the counting of pulses from CD4045AE and will require 24 hours to calibrate the system again on a negative transition.

A pulse counter has been designed to jam the DE4020 with necessary pulses to calibrate the system at any time desired.

Table 3. C5 Calibrator Parts List

C1	Capacitor 15-60pf	Erie 0538011F15-60
C2	Capacitor 25pf	Sprague 10TCC-Q25 NPO
C3,5,7,11	Capacitor 0.47uf	Erie 8131-050-651-224M
C4,6,8	Capacitor 4.7uf	Sprague 196D475X9010HA1
C9	Capacitor 0.22uf	Erie 8131-050-651-224M
C10	Capacitor 0.27uf	Aerovox CK06BX274K
C12	Capacitor 68uf	Kemet T362C686K015AS
C13	Capacitor 6.8uf	Sprague 196D685X9010HA1
R1	Resistor 15 meg ohm	1/4W 5%
R2	Resistor 1k ohm	1/4W 5%
R3	Resistor 110k ohm	1/4W 5%
R4,27	Resistor 20k ohm	1/4W 5%
R5,7,14	Resistor 200k ohm	1/4W 5%
R6,8	Resistor 2 meg ohm	1/4W 5%
R9,10,16	Resistor 27k ohm	1/4W 5%
R11,13,17	Resistor 110 ohm	1/4W 5%
R12	Resistor 330 ohm	1/4W 5%
R15	Resistor 5.1 meg ohm	1/4W 5%
R18	Resistor 20.0k ohm	RN55D 1%
R19	Resistor 5.36k ohm	RN55D 1%
R20	Resistor 698 ohm	RN55D 1%
R21	Resistor 75 ohm	RN55D 1%
R22	Resistor 9.31k ohm	RN55D 1%
R23	Resistor 665 ohm	RN55D 1%
R24	Resistor 562 ohm	RN55D 1%
R25	Resistor 200 ohm	1/4W 5%
R26	Resistor 180k ohm	1/4W 5%
R28,34	Resistor 33k ohm	1/4W 5%
R29	Resistor 1.2 meg ohm	1/4W 5%
R30	Resistor 560k ohm	1/4W 5%
R31	Resistor 6.8k ohm	1/4W 5%
R32	Resistor 36k ohm	1/4W 5%
R33	Resistor 75k ohm	1/4W 5%
R35	Resistor 10k ohm	1/4W 5%
Cr1,2,3	Diode	1N914
Q1,2,3,4	Transistor, Darlington	Motorola MPS A 14
IC1	Digital Integrated Circuit	RCA CD4045AE
IC2	Digital Integrated Circuit	RCA CD4020AE
IC3	Digital Integrated Circuit	RCA CD4049AE
IC4	Digital Integrated Circuit	RCA CD4001AE
IC5	Digital Integrated Circuits	RCA CD4011AE
IC6	Digital Integrated Circuit	RCA CD4021AE
RY1A,2,3	Relay	Magnecraft W172DIP5
RY1B	Relay	Magnecraft W171DIP7
RY4	Relay	Magnecraft W171D1P25
X1	Crystal	Monitor Products 397.682KHz
	IC Socket 2 ea	Amphenol 821-25011-144
	IC Socket 4 ea	Amphenol 821-25011-164
	Battery 5.6V	Mallory TR234
	Battery 9V	Mallory NM1604
	Battery 1.35V	Mallory TR233R (use 1 cell with cover)
	Connector 5 pin	W.S. Deans 5 pin

C-5 CALIBRATOR

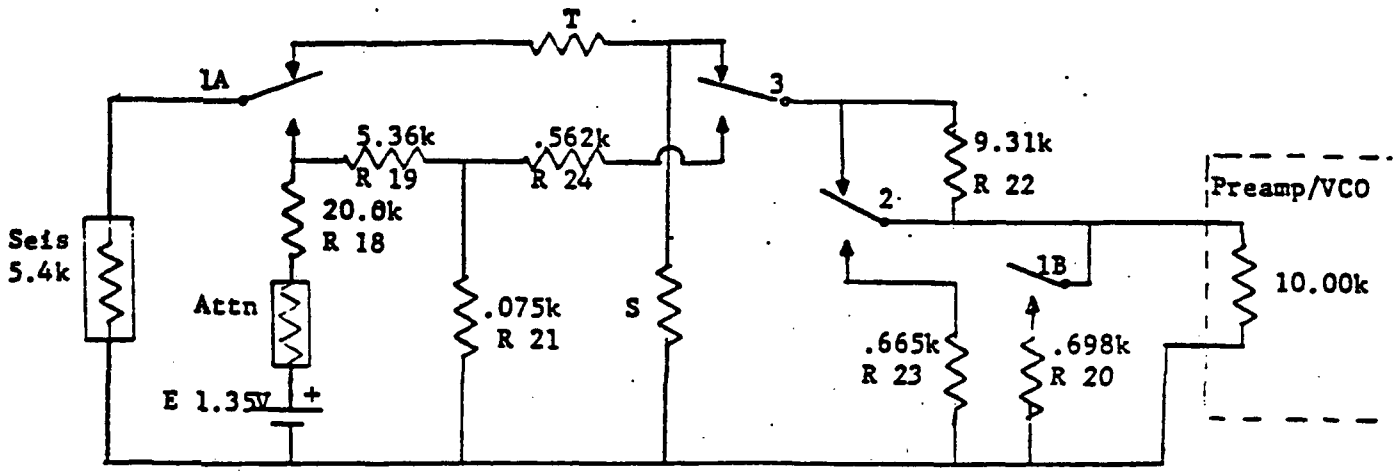
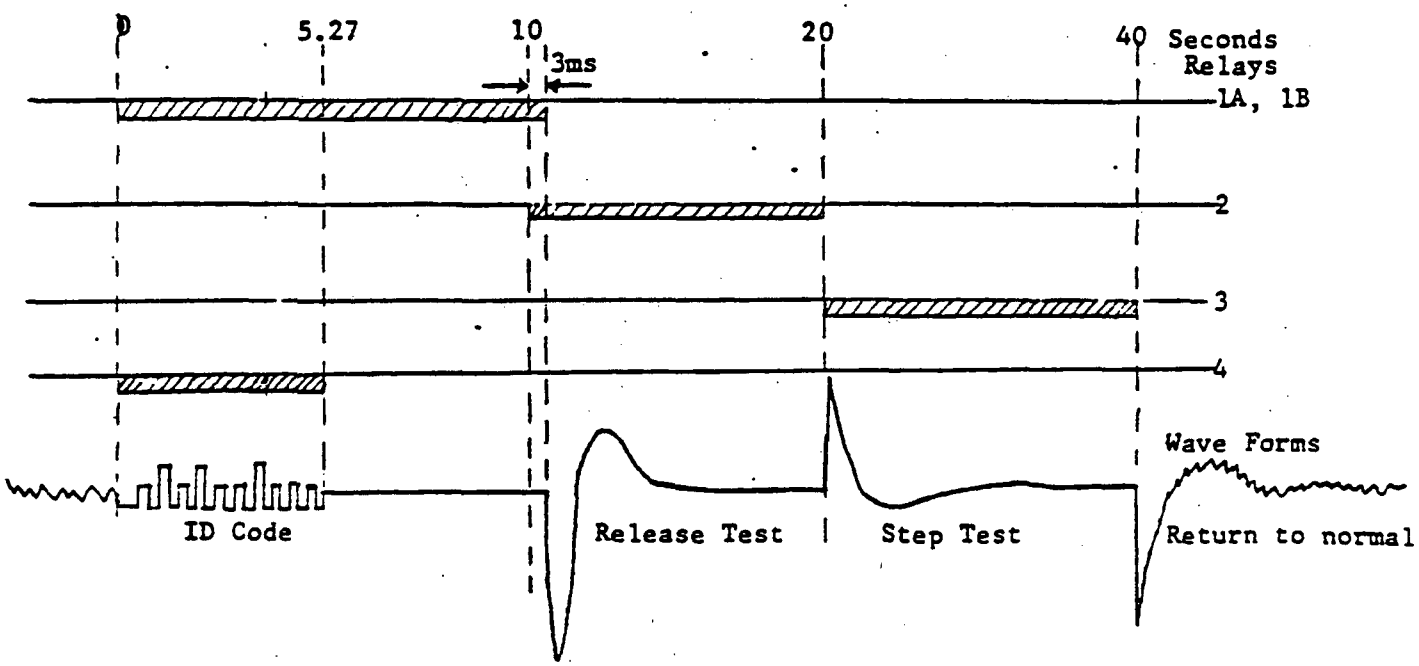


Figure 1a



Step 1 a Seismometer mass offset (ID code sent directly to VCO input)

b Amplifier terminated to preserve impedence balance

Step 2 a 24Db pad inserted in line to preamp input

b Mass released 3ms later

Step 3 a Voltage step applied to preamp input

b Station returned to normal operation

Figure 7

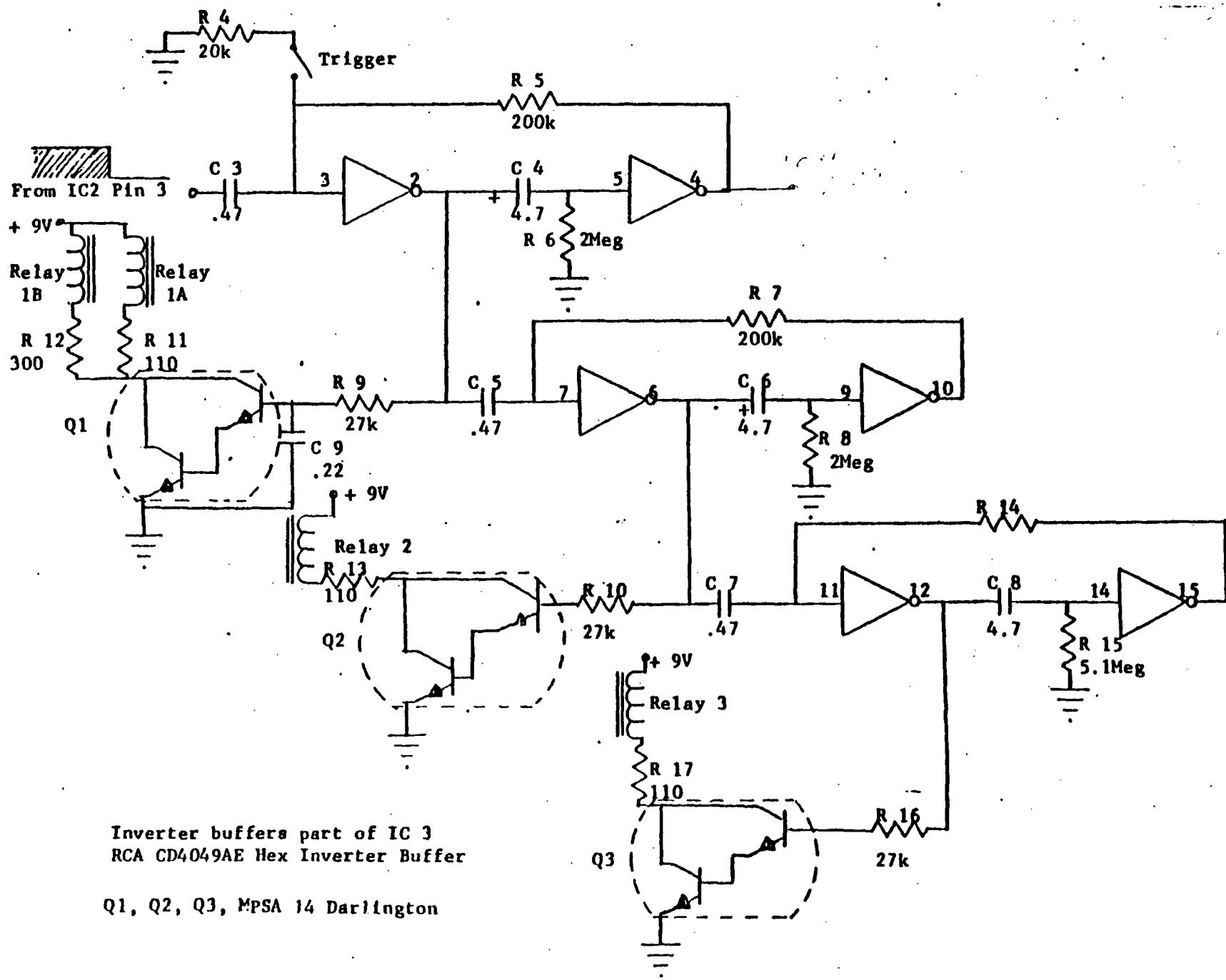
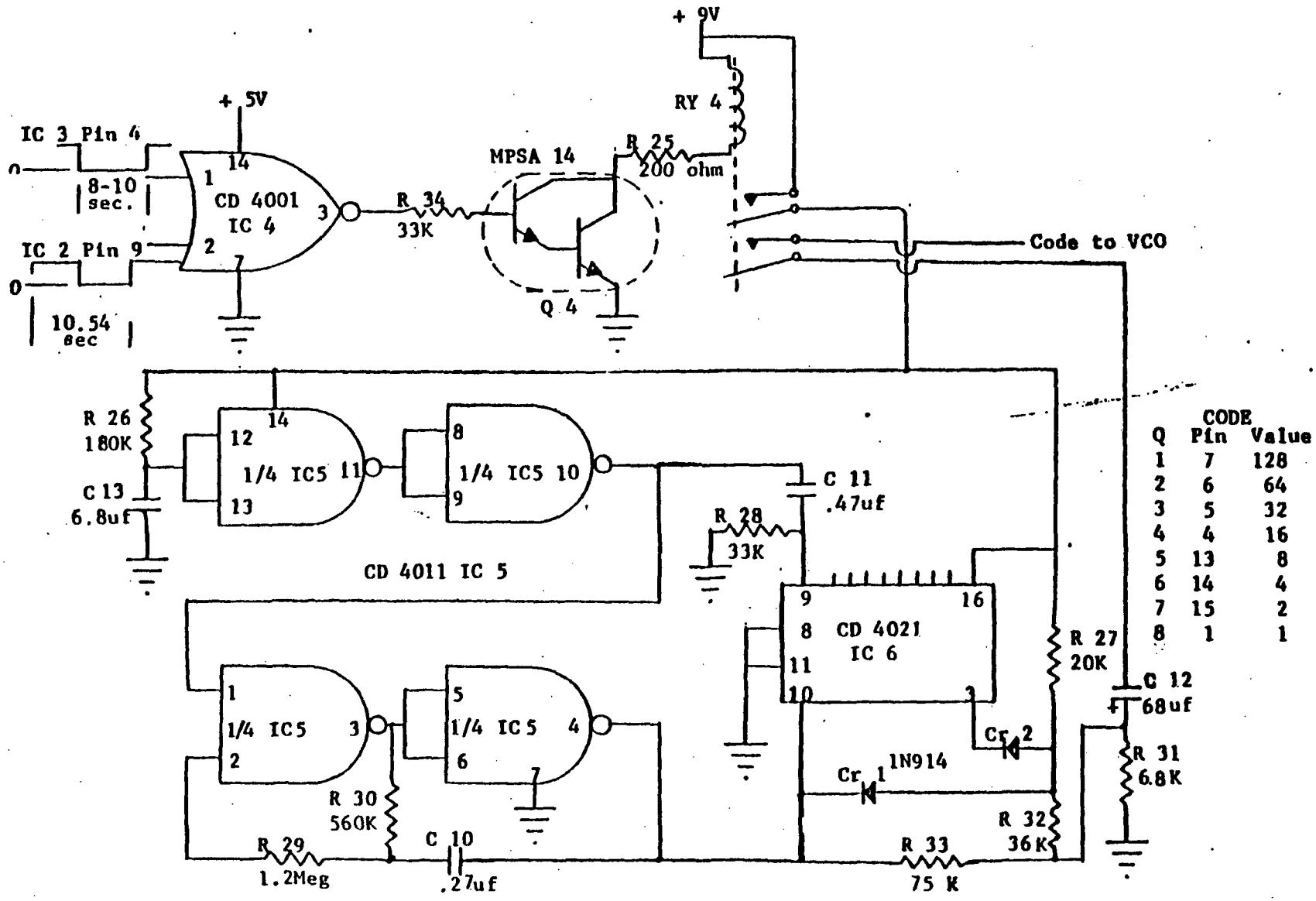


Figure 8 Schematic diagram of relay control circuit C-5 Calibrator



Code Identification Circuit, C5 Calibrator

FIGURE 9

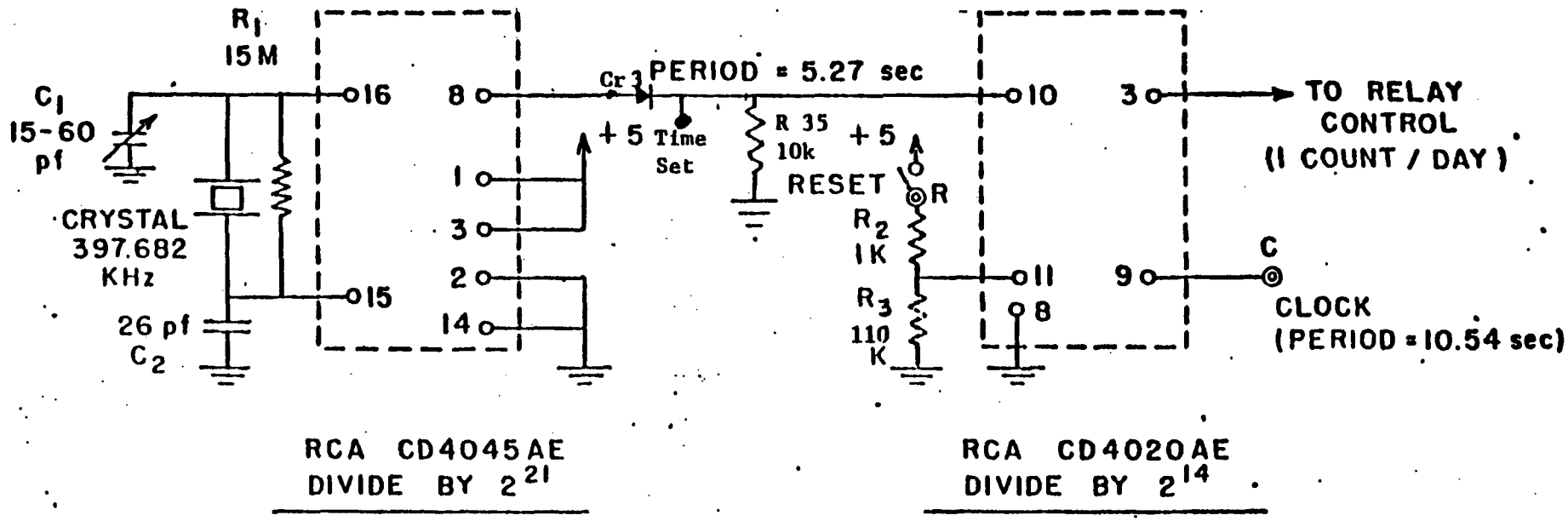


Figure 10 -- Clock circuit. C-5 Calibrator

C1 3
K-5 10K

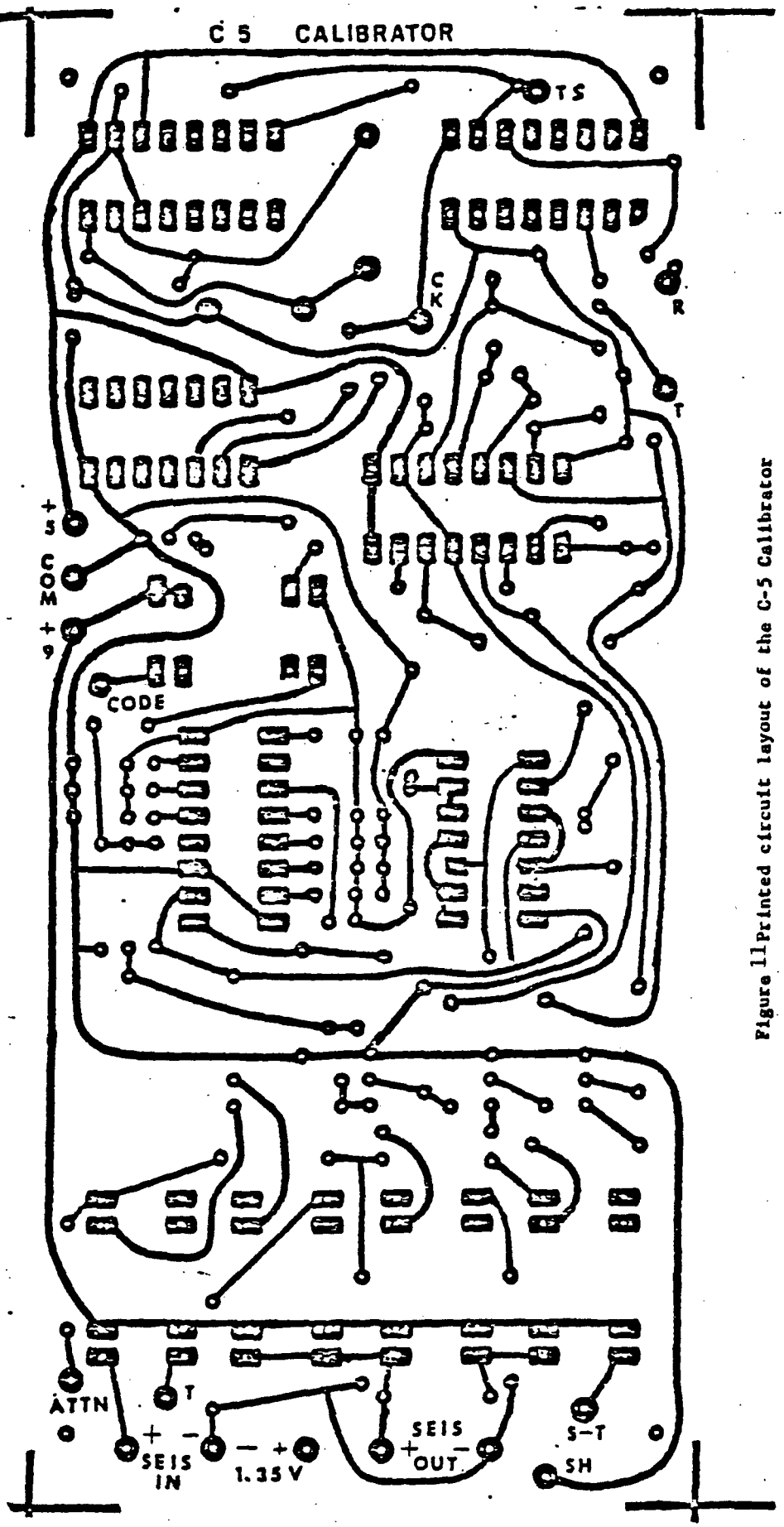


Figure 11 Printed circuit layout of the C-5 Calibrator

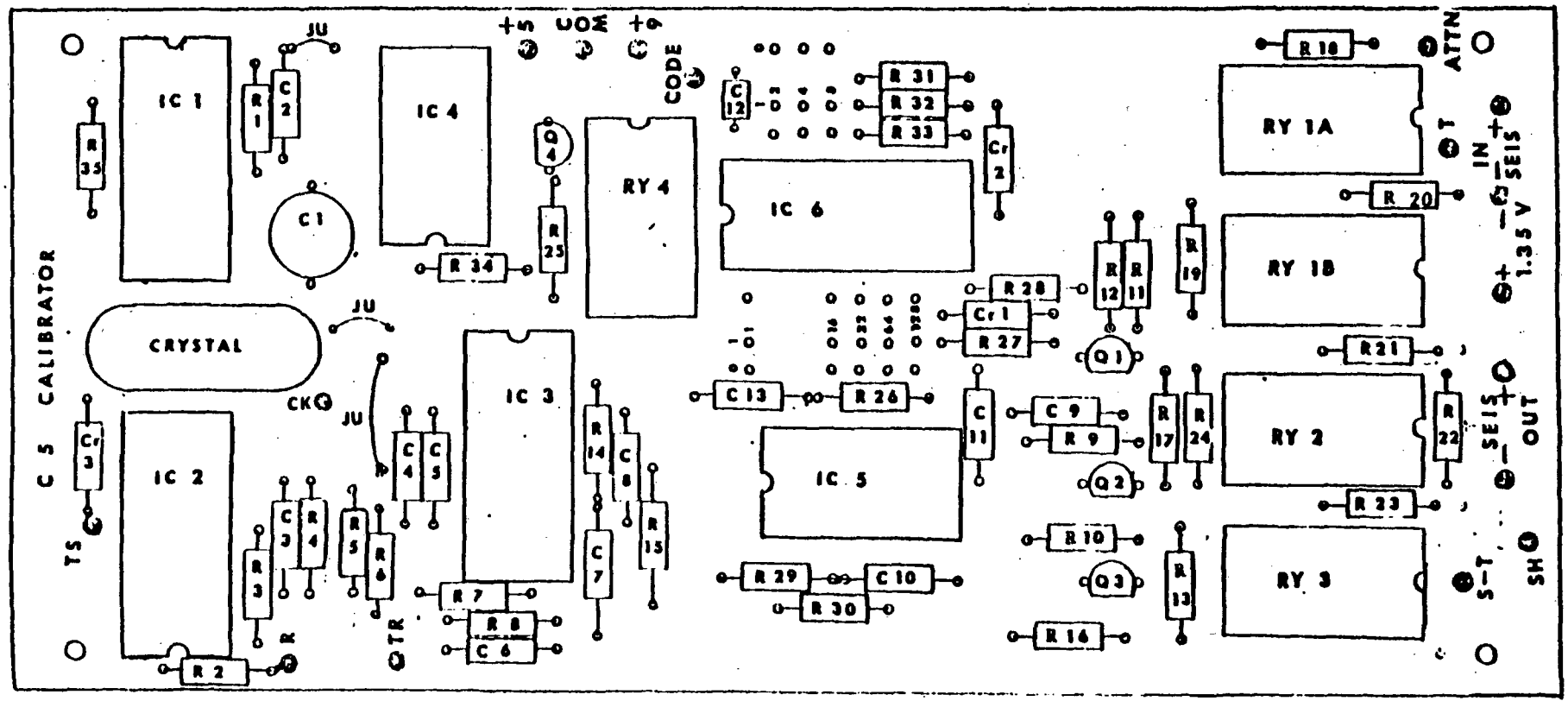


Figure 12 Componant lay out

References Cited

Jensen, G. E., 1977, Crystal VCO center frequency stabilizer, U.S. Geological Survey Open-file Report 77-184, 9 p.

Van Schaack, J., 1975, Self-calibrating seismic amplifier and telemetry system: U.S. Geological Survey Open-File Report, 20 p.

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CRYSTAL VCO CENTER FREQUENCY STABILIZER

-by

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Open-File Report

#77-184

CRYSTAL VCO CENTER FREQUENCY STABILIZER

PURPOSE

This device is designed to maintain a constant center frequency in NCER seismic voltage-controlled oscillators (VCO's). The center frequency of the current VCO design without this stabilizer can drift as much as ±30 hertz from the preset center frequency. The drift can be caused by various factors including temperature, aging and change in battery voltage. The stabilizer will maintain the preset center frequency independent of the cause.

THEORY

The principle behind the stabilizer is the introduction at the VCO input of a DC correction voltage which compensates for any center frequency drift. The scheme requires an accurate method of measuring the center frequency. This requirement is hampered by the fact that a seismic signal is constantly applied to the VCO input. Therefore the output rarely if ever rests at the center frequency long enough to measure it directly. The center frequency can be measured indirectly though. Since the seismic signal is AC coupled, it has no DC component of its own. So if the frequency is measured over a long time period relative to the seismic frequencies it will average out to the center frequency. Since center frequency drifts occur on the order of minutes, hours, and days and seismic signals have periods of a few seconds or less, about a 10-second frequency measurement period is appropriate. After each frequency measurement is made the DC correction voltage is increased

or decreased depending on whether the center frequency is low or high respectively. The correction voltage change is so small (-54db) that it is not apparent above system noise but after a period on the order of a few minutes these small changes will add up to a significant correction.

DESIGN

As described above this device incorporates two main components. One component measures the center frequency. The other component produces a DC correction voltage. Also included is a small amount of logic to control these components. In the schematic in figures 1 and 2, IC1 and IC2 are 8-bit binary down counters connected to produce a 16-bit down counter. This is the frequency measuring section. A 10.54 second period signal from the calibrator crystal is the time reference for this section. IC7 and IC8 are 4-bit binary up-down counters connected to produce an 8-bit up-down counter. The outputs of this counter are connected to an R-2R ladder digital-to-analog converter. Together these constitute the correction voltage generator.

The logic sequence is as follows. A square wave with a period of 10.54 second and which is crystal controlled is the input of IC6. The output of IC6 is the same square wave at a voltage level which is compatible with the rest of the system (since the VCO and calibrator are on separate battery systems). The rising edge of this square wave triggers the one-shot IC5b whose output lasts 100 μsec. The falling edge of this signal triggers one-shot IC5a whose output also lasts 100 μsec. This signal sets flip-flop IC4a and also sets a count into the 16-bit down counter. This count is equal to the number of cycles the VCO center frequency will

put out in 10.54 seconds. Then every cycle of the VCO decrements this counter one count. When the count equals zero the counter outputs a pulse which is inverted by IC3a to reset flip-flop IC4a. The output of this device determines whether the 8-bit up-down counter counts up or down.

Now, if the next rising edge of the square wave occurs before the down counter reaches zero, flip-flop IC4a will not be reset and the output pulse of one-shot IC5b will clock the 8-bit up-down counter causing it to count up one count. This results in a small voltage increase (~12 mv) at the VCO code input. This is what is needed since the fact that the 16-bit down counter did not reach zero in 10.54 seconds indicates the center frequency is low.

If the 16-bit counter does reach zero before the next square wave rising edge the flip-flop will be reset causing the clock pulse to decrement the 8-bit counter. This produces a decrease in voltage to correct for a high center frequency indicated by the 16-bit counter reaching zero in less than 10.54 seconds.

The section including IC3c and IC3d produces a pulse upon power-up which sets a count into the 8-bit counter to produce zero correction voltage. Another feature is the section including IC3b and IC4b which prevents any change in the correction voltage once the 8-bit counter has reached the upper or lower end of the range.

Since the correction counter is 8-bit there are a total of 256 correction steps possible. Each step produces a center frequency change of about 0.5 hertz. This corresponds to about -54 db relative to full scale modulation of $\pm$125 hz. With a correction step of .5 hertz the maximum amount of correction is approximately $\pm$63 hertz.

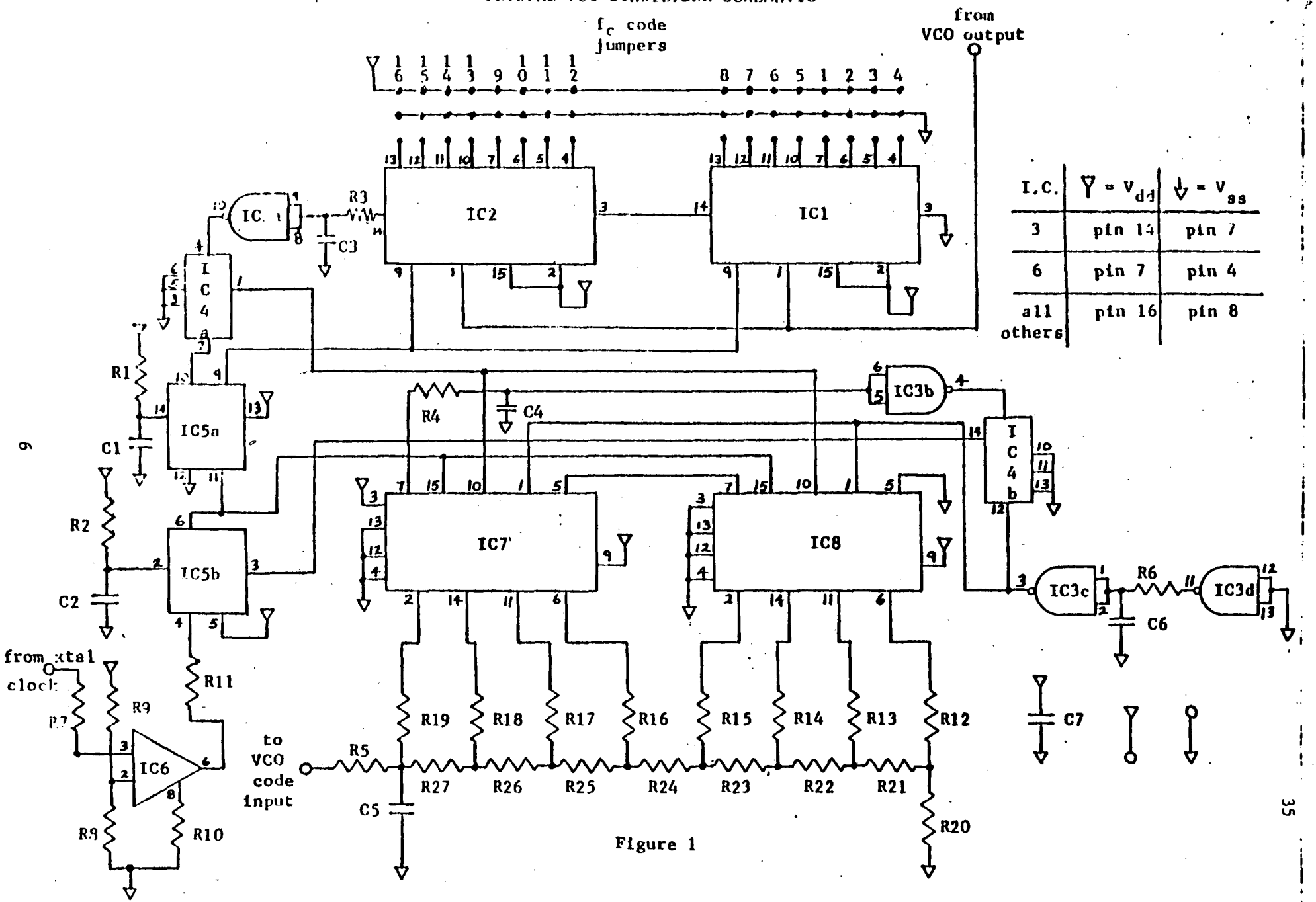
When the stabilizer is connected there is a large decrease in frequency, initially, due to the current draw of the reset pulse. After this the frequency will return to a few hertz below the original frequency. If the voltage at the code input to the VCO is measured relative to common, it should be within a few tens of millivolts of zero volts. Every 10.54 seconds it will change approximately 12 millivolts. This amount can vary a few millivolts from step to step. If the frequency is below the preset center frequency the change should be positive. If it is above the change should be negative. At the same time the frequency will change in the same direction at a rate of about 1 hertz every 20 seconds. When the frequency reaches the preset center frequency the correction voltage will be observed to change direction every step, first increasing then decreasing. Occasionally the voltage will go two steps in one direction as the stabilizer corrects for drift.

This device was designed to allow retrofitting to existing seismic VCO's. Figure 3 shows the layout of the stabilizer board which mounts over the calibrator board and is connected by a 5-pin plug. How the stabilizer is set for the desired center frequency is shown in figure 4. This jumper code is the only change necessary for frequency. All parts are the same for every frequency.

The stabilizer has been field tested and the design refined. The unit uses about 25-40 ua. of current after initialization. A few precautions should be taken to ensure proper operation. First, disconnect the stabilizer while setting the calibrator time. Always leave the stabilizer disconnected for at least 10 seconds to allow the reset capacitor to discharge. Finally, since there are two 5-pin female sockets on the

calibrator side of the electronics package be sure to connect the stabilizer to the one with five (instead of four) wires attached to it.

CRYSTAL VCO STABILIZER SCHEMATIC



I.C.	▽ = V_{dd}	▽ = V_{ss}
3	pin 14	pin 7
6	pin 7	pin 4
all others	pin 16	pin 8

Figure 1

CRYSTAL VCO STABILIZER PARTS LIST

C1, 2	Capacitor .01 µf	Arco TCD 103v
C3, 4, 5	" 680 pf	Kemet C320C681K1G5CA
C6	" .1 µf	" C330C104M5U5EA
C7	" 15 µf	" T362B156K0ZAS
IC1, 2	CMOS integrated circuit	RCA CD40103BE
IC3	" " "	" CD4011AE
IC4	" " "	" CD4027AE
IC5	" " "	" CD4098BE
IC6	Linear " "	National LM4250CN
IC7, 3	CMOS ' '	RCA CD4029AE
R1, 2	Resistor 6.8 KΩ	1/4 W 5%
R3, 4	" 24 KΩ	" "
R5	" 100 Ω	" "
R6	" 22 MΩ	" "
R7, 8	" 10 MΩ	" "
R9	" 5.1 MΩ	" "
R10	" 2 MΩ	" "
R11	" 1 KΩ	" "
R12-20	" 560 KΩ	" "
R21-27	" 270 KΩ	" "

DIL socket, 16 Pin, 6 ea.	Amphenol 821-20012-164
DIL socket, 14 Pin, 1 ea.	" 821-20012-144
DIL socket, 8 Pin, 1 ea.	" 821-20012-084
Connector, 5 Pin, 1 ea.	W. S. Deans

Figure 2

CRYSTAL VCO
STABILIZER
LAYOUT

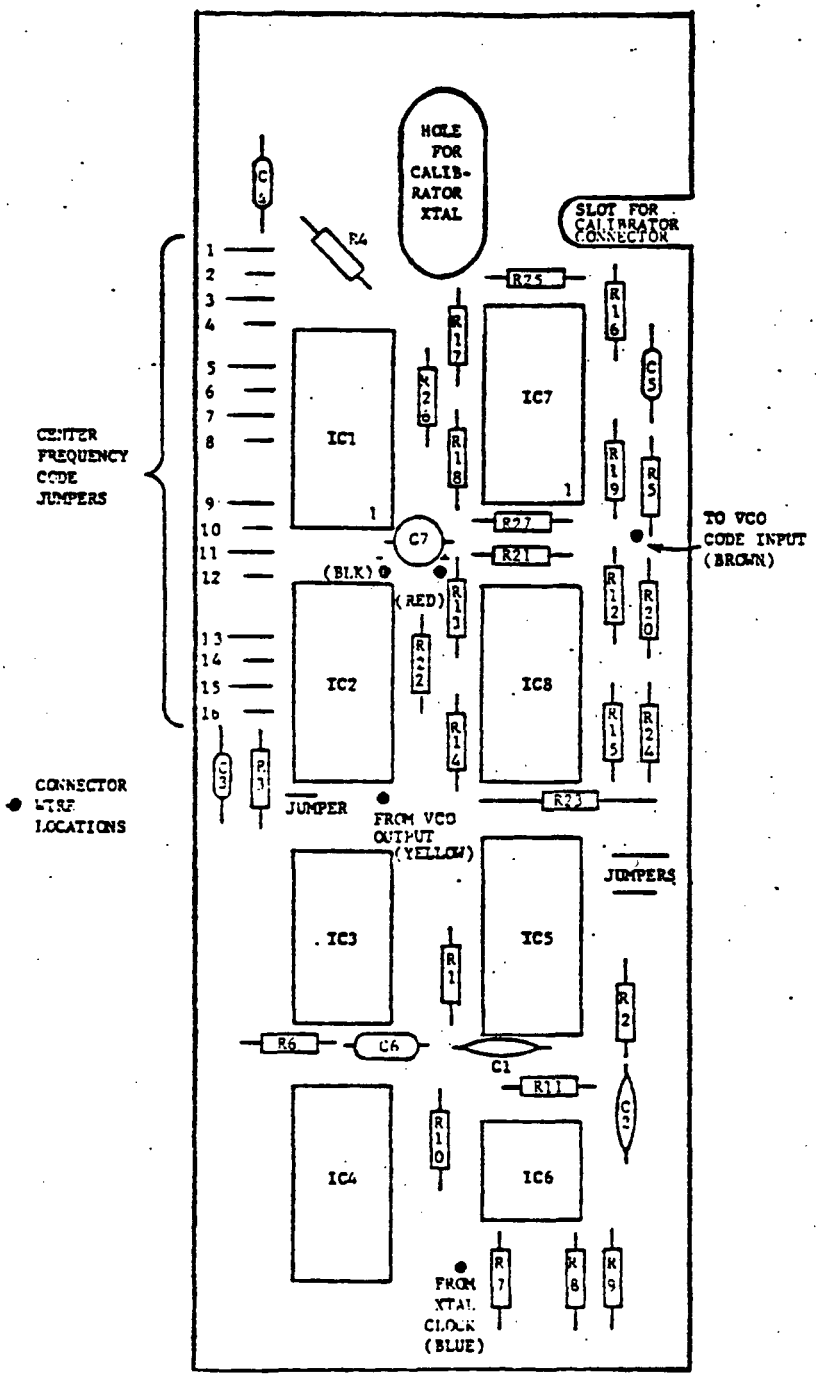
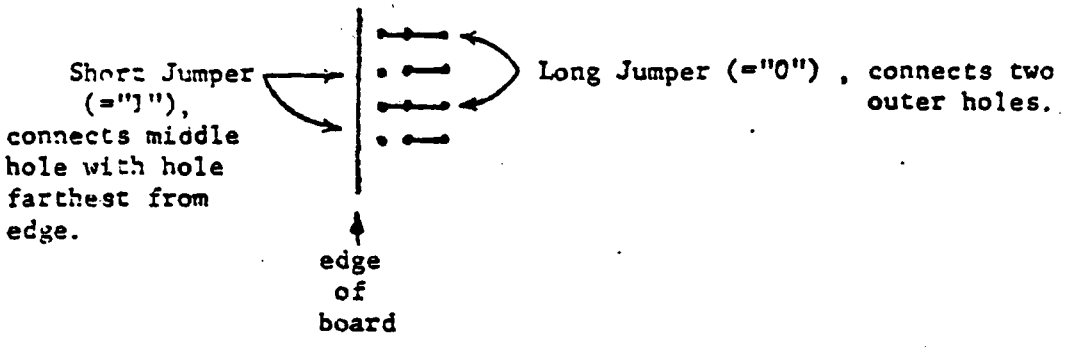


Figure 3

CENTER FREQUENCY JUMPER CODE



Center Frequency (hz.)	Short Jumpers (All others long)
680	2,9,10,13
1020	2,3,9,11,14
1360	1,9,13,14
1700	1,3,10,11,15
2040	1,2,10,13,15
2380	1,2,3,11,14,15
2720	5,13,14,15
3060	4,5,9,11,13,14,15,10

To find the code for other center frequencies, multiply the center frequency by 10.547. Round this number to the nearest integer and then calculate its binary equivalent. Apply this number to the jumper code according to the order below using a short jumper for a "1" and a long jumper for a "0".

Binary Bit	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Jumper	16	15	14	13	9	10	11	12	8	7	6	5	1	2	3	4

Figure 4